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par

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Conception et modélisation de la répartition de l'horloge des systèmes intégrés par voie optique

Soutenue le 28 Janvier 2004 devant la commission d'examen :

Composition du jury

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THESE

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Master of Science TU Lodz

Design and Modeling of Optical Clock Distribution Networks in Integrated Systems

Defended on January 28, 2004 before examination commission :

Composition of jury

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[3] Laboratory for Microelectronics Technologies in National Center for Scientific Research, Grenoble

[4] Laboratory of Electromagnetism, Microondes and Optoelectronic in National Polytechnic Institute of Grenoble

[5] Institute in Microwaves and Optics Communications Limoges

[6] The Institute of Fundamental Electronics, Orsay.

[7] Materials Physics Laboratory in Scientific and Technical University of Lyon.

[8] Polish Committee for Scientific Research

Avertissement

Le Conseil Scientifique de l'Ecole Centrale de Lyon du 6 Octobre 2003 a adopté une délibération autorisant, dans le cadre d'une thèse en co-tutelle, l'usage de la langue anglaise pour la rédaction du manuscrit. Dans ce cas un résumé étendu en français doit accompagner le manuscrit. Dans ce résumé (pages viii à xxii), les références se rapportent bien sûr au texte principal.

Warning

The Scientific Council of Ecole Centrale de Lyon of October 6, 2003 adopted a deliberation authorizing, within the framework of a thesis in Co-supervision, the use of the English language for the drafting of the manuscript. In this case a extended summary in French must accompany the manuscript. In this summary (pages viii to xxii), the references are referred of course to the main text.

Chapitre I

Motivation

Les progrès de la technologie de fabrication des circuits intégrés rendent possible la fabrication de puces contenant des millions de transistors fonctionnant à plusieurs gigahertz. Si ces progrès continuent au même rythme, des circuits contenant plusieurs centaines de millions de transistors seront fondus dans quelques années. Cependant, il est clair que les procédés de la microélectronique tendent vers des limites physiques toujours plus difficiles à repousser.
Les progrès de la microélectronique sont dus pour l'essentiel à la réduction de la taille des transistors élémentaires. Cependant, alors que la diminution du paramètre technologique améliore le comportement des composants actifs (les transistors), elle conduit en général à une augmentation des délais de propagation et de la puissance consommée dans les interconnexions. Ainsi, pour les technologies actuelles, le temps de transport de l'information sur les pistes d'interconnexion domine sur le temps de commutation des portes logiques. Même si de nouveaux matériaux apparaissent, il est certain que les interconnexions constituent dès à présent un goulot d'étranglement sur le chemin de performances accrues. L'utilisation de l'optique est une des alternatives potentielles qui permettront de lever les verrous imposés par les interconnexions métalliques ; cependant, bien évidemment, cette alternative n'est crédible que si elle apporte un gain de performances appréciable.
Le but de ce travail est de permettre une comparaison sans ambiguïté des performances d'un réseau de distribution classique de l'horloge des circuits intégrés avec celles d'un réseau optique.

Chapitre II

Evolution technologique

2.1 *Introduction*

D'après l'ITRS, les progrès des performances des circuits intégrés continueront, dans les quinze ans à venir, au même rythme que lors des 40 dernières années. Cependant, pour atteindre ce but, de nouvelles technologies devront être mises en œuvre

Si la réduction de taille des composants actifs élémentaires conduisent à l'amélioration des performances des CI (densité et vitesse de fonctionnement), la réduction de taille des interconnexions conduit à une augmentation de leur densité mais au prix d'une augmentation des délais de propagation et de la puissance consommée.

Ce chapitre présente les conséquences de la réduction des tailles des structures élémentaires.

2.2 *Transistor scaling*

Le tableau 2-1 présente les différents scénarios de réduction des dimensions des transistors CMOS.

Le premier scénario, appelé "*full scaling*" suppose que les dimensions et les tensions (tensions de seuil des transistors et tensions d'alimentation) sont réduites d'un facteur S. Le second suppose que seules les dimensions sont réduites du facteur d'échelle S. Et enfin, le scénario dit "*general scaling*" suppose que les dimensions sont réduites d'un facteur S alors que les tensions sont divisées par U.

Le tableau 2-2 donne les caractéristiques principales de la technologie CMOS pour la décennie à venir: les performances ainsi que la densité d'intégration continueront donc de croître, cependant, de nombreuses limites (pratiques ou fondamentales) nécessiteront

2.3 *Interconnect scaling*

Les performances des circuits intégrés sont de plus en plus déterminées par celles des interconnexions. Aussi, est-il particulièrement souhaitable de prévoir quelles seront les contraintes pesant sur les interconnexions pour les technologies futures.
La loi empirique de Rent relie le nombre de connexion d'un bloc fonctionnel au nombre de sous-blocs qui le constituent:
$T=kN^p$
Où T est le nombre de connexions d'un bloc fonctionnel, N, le nombre de portes le constituant et p est l'exposant de Rent caractéristique de la complexité du routage.

A partir de la loi de Rent, il est possible de déterminer la distribution de la longueur des liens dans un système intégré [DAV-98; KAN-90]. La figure 2-5 met en évidence la répartition des interconnexions en deux familles:

-les interconnexions locales qui relient des portes à très courte distance. Leur longueur décroît avec le paramètre technologique, elles sont en général routées sur les premiers niveaux métalliques.

-les interconnexions globales dont la longueur est de l'ordre de grandeur de la dimension du circuit. Elles ont routées sur les niveaux métalliques supérieurs où les pistes conductrices peuvent être épaisses et larges afin de réduire la résistance linéique.

La figure 2-6 montre la structure générale du réseau d'interconnexion. Les interconnexions locales sont réalisées sur les niveaux métalliques les plus proches du silicium, les interconnexions globales sur les niveaux les plus élevés. On notera que la largeur et l'épaisseur des pistes métalliques augmentent des couches basse aux couches élevées (*reverse scaling*).

L'augmentation des performances fréquentielles des circuits conduit à une augmentation du nombre de couches métalliques.
En effet, les contraintes temporelles sur la propagation des signaux amènent à réduire la résistance (R) et la capacité linéiques (C) des interconnexions et donc à augmenter l'épaisseur et la largeur des pistes métalliques pour réduire R et à augmenter la distance entre les pistes afin de réduire C. L'encombrement du réseau d'interconnexion augmente donc (essentiellement pour les interconnexions globales), la connectabilité est assurée par une augmentation du nombre de couches métalliques.
Le tableau 2-5 donne les prévisions de l'ITRS pour les principaux paramètres des interconnexions métalliques. On notera en particulier l'augmentation du nombre de couches de métallisation et celle des retards de propagation.

2.4 *La crise des interconnexions*

2.4.1 Consommation de puissance

L'augmentation de la fréquence de fonctionnement des circuits et de la densité d'intégration conduit à un accroissement de la puissance électrique consommée. Ainsi, par exemple, certains microprocesseurs peuvent avoir à dissiper plus de 100W. La densité de puissance que cela représente devient une limite à l'augmentation des performances et de la complexité.

2.4.2 Temps de propagation

La figure 2-10, issue de l'édition 2001 de la feuille de route de l'ITRS, montre l'évolution relative des temps de propagation dans les portes et dans les interconnexions avec les générations technologiques successives.
L'amélioration des matériaux (en particulier des diélectriques inter-couches métalliques) ne permettra pas d'atteindre les performances requises pour les liens globaux.

2.4.3 Débit global

Le débit global d'un réseau d'interconnexions métalliques est limité [MIL-97]: $B \approx B_0 \frac{A}{L_{int}^2}$, expression empirique dans laquelle A est la surface totale de conduction et L_{int}, la longueur du lien, B_0 est une constante dépendant de la technologie, valant environ 10^{16} dans le cas des circuits intégrés. Il est à noter que le débit ne

varie pas avec le facteur d'échelle, et que, donc, les interconnexions électriques classiques ne pourront pas assumer des débits de l'ordre du térabit par seconde.

2.5 *Solutions potentielles*

2.5.1 Les matériaux conducteurs

Pour les technologies les plus avancées, les interconnexions métalliques sont réalisées en cuivre. Le cuivre a une résistivité de 1,7 10^{-8} □m. Cependant, les barrières diélectriques nécessaires pour éviter la diffusion du cuivre lors du process technologique conduisent à une résistivité apparente de l'ordre de 2,2 10^{-8} □m. Il n'existe pas de matériau métallique qui permette d'envisager une alternative à l'usage du cuivre.

2.5.2 Matériaux diélectriques

La réduction de la constante diélectrique des matériaux permettant d'isoler les pistes métalliques permet de réduire la capacité linéique des interconnexions et donc de réduire les temps de propagation. Néanmoins, même si des matériaux diélectriques à constante voisine de 2 sont utilisés dans l'avenir, la capacité linéique sera réduite d'environ 50%, ce qui ne permettra pas d'atteindre les spécifications voulues.

2.5.3 Solutions alternatives

Il est établi que les interconnexions métalliques classiques ont atteint ou approchent leurs limites fondamentales et présentent un goulot d'étranglement sur la voie de l'augmentation des performances des systèmes intégrés. Les évolutions technologiques concernant les matériaux ne permettront pas de résoudre ce problème, aussi des solutions révolutionnaires doivent elles être étudiées.
Parmi ces solutions innovantes, le concept d'interconnexion optique apparaît comme une alternative prometteuse pour résoudre les problèmes des interconnexions globales.

2.6 *Conclusion*

Ce chapitre, fondé sur les prévisions de l'ITRS, a mis en évidence les conséquences de la diminution du paramètre technologique sur les performances (puissance, retard, densité) des interconnexions globales: les interconnexions métalliques atteignent leurs limites et constituent un des défis majeurs pour l'amélioration des performances globales des circuits.

Chapitre III

Réseau de distribution d'horloge électrique

3.1 *Introduction*

Le réseau de distribution d'horloge répartit le signal d'horloge à tous les composants de synchronisation d'un circuit. L'intégrité du signal d'horloge doit être respectée et les paramètres de retard relatif (*clock skew*), de pente des fronts d'horloge (*clock slew rate*), de retard de phase et de sensibilité aux variations technologiques et environnementales doivent être maîtrisés. De plus, ces objectifs doivent être atteints en minimisant les ressources de surface occupée et de puissance consommée.
L'arbre d'horloge des microprocesseurs modernes peuvent consommer jusqu'au tiers de la puissance totale dissipée par le circuit et conditionne sa vitesse de travail maximale.

3.2 *Les paramètres de la distribution d'horloge*

Ce paragraphe présente les principaux paramètres permettant de qualifier la distribution d'horloge.

3.2.1 Retard relatif (*Clock skew*)

De façon générale, un système numérique est constitué d'éléments de synchronisation (registres) entre lesquels un bloc combinatoire traite le signal. La figure 3-1 présente une partie du chemin de données [FRI-95]. C_i et C_j sont les signaux d'horloge pilotant les registres successifs R_i et R_j.

La fréquence maximale de travail f_{CLKmax} avec laquelle les données peuvent être traitées est donnée par:

$$\frac{1}{f_{CLK\,max}} = T_{CP\,min} \geq T_{Skew} + T_{PD} \quad (3.1)$$

expression dans laquelle, T_{CPmin} est la période d'horloge minimale, T_{Skew} est le retard relatif des fronts d'horloge et T_{PD} est le retard total entre deux registres.

T_{PD} est la somme du temps de retard entre l'arrivée du front d'horloge et l'instant où la donnée est établie à la sortie du registre (T_{CLK-Q}), des temps de propagation dans le bloc logique (T_{logic}), et les interconnexions (T_{int}) et du temps d'acquisition du registre de sortie $T_{(set-up)}$.

Le *clock skew* est défini comme le retard relatif maximal entre les instants des fronts d'horloge pilotant deus registres successifs (fig. 3-2).

Comme l'indique l'équation 3.1, le *clock skew* peut limiter considérablement la fréquence maximale d'utilisation d'un système synchrone.

Sources du *skew*:
Une des gageures à tenir dans la phase de conception de la distribution d'horloge est de limité le *clock skew*. L'ordre de grandeur du *skew* acceptable est de l'ordre de 10% de la période d'horloge. Les origines du *skew* sont multiples, on peut citer (WAN-83):

-la différence de longueur du lien entre la source de l'horloge et les registres
-la différence de délais dans les *buffers* sur les chemins entre la source et les registres
-les différences entre les paramètres technologiques des différents chemins (résistance linéique, capacité linéique, dimension des lignes...
-les différences de paramètres électriques des composants actifs (tensions de seuil, mobilité...).

Il ets donc clair que, pour limiter le *clock skew* les chemins entre la source d'horloge et les registres doivent être équilibrés.

3.3.2 Consommation de puissance

La dissipation de puissance dans l'arbre d'horloge lui même est l'autre paramètre principal à optimiser. Le réseau de distribution de l'horloge peut en effet, dissiper jusqu'à 30% de la puissance totale consommée par le circuit.

3.3 *Conception du réseau de distribution d'horloge (RDH)*

Très souvent, le réseau de distribution d'horloge utilise des arbres et des grilles (fig. 3-6). Le RDH comprend en général, une boucle à verrouillage de phase, un arbre global qui distribue le signal sur la surface du circuit (cet arbre global est routé sur les niveaux de métallisation les plus élevés), éventuellement un arbre secondaire (routé sur les couches intermédiaires), et des réseaux locaux (en général, sous forme de grilles) qui transportent le signal d'horloge jusqu'aux registres.

3.3.1 Les arbres de distribution

La stratégie la plus couramment admise pour distribuer l'horloge est d'utiliser un arbre équilibré (fig. 3-7). Pour contrôler au mieux le temps de propagation sur les lignes constituant l'arbre, chaque ligne est entourée de lignes d'alimentation (fig. 3-8).

3.3.2 Les arbres amplifiés

Dans le but de réduire les distorsions subies par le signal d'horloge et de minimiser le temps de propagation sur les branches, des *buffers* sont insérés régulièrement sur les lignes constituant l'arbre (fig. 3-9).
L'insertion de *buffers* contribuent à accroître les ressources matérielles utilisées et on cherche généralement à minimiser le nombre de *buffers*:

-les *buffers* donnent naissance à une nouvelle source de skew,
-le nombre total de *buffers* peut être assez grand pour augmenter de façon appréciable la surface du circuit,

-la puissance totale consommée dans le RDH dépend pour une bonne part du nombre de *buffers*.

3.3.3 Structure des arbres de distribution d'horloge

3.3.3.1 Grille

La grille est la structure la plus simple: une grille conductrice est alimentée par des *buffers* (fig. 3-10).
Les avantages de cette structure résident dans sa régularité, sa granularité (tous les points du circuit sont aisément atteints), sa robustesse aux variations technologiques, la facilité de sa conception. Son inconvénient principal tient au fait que cette structure est très capacitive et donc, consommatrice d'énergie.
Les grilles sont classiquement utilisées comme étage final du RDH.

3.3.3.2 Arbre en H symétrique

Le *skew* étant essentiellement dû au déséquilibre des temps de propagation dans les différentes branche du RDH, une structure symétrique en H (fig. 3-11) ou, plus rarement en X, permet de le minimiser.
Dans une structure en H, le *skew* est dû principalement aux variations technologiques des paramètres électriques des branches.

3.4 *Exemples d'implémentation*

De nombreux exemples de RDH utilisés dans des microprocesseurs extrêmement populaires ont été publiés, le tableau 3-1 résume les principales architectures et leurs principales performances.

3.4.1 Microprocesseur 21264 Alpha

La famille des processeurs Alpha de DEC ont évolué au cours de la dernière décennie d'une fréquence de 200 MHz en 1992 à 1,2 GHz en 2001. La troisième génération de processeurs Alpha (codés 21264) fonctionnent à 600MHz et ont été réalisés avec une technologie 0,35µm (1998), c'est le premier microprocesseur de sa famille à mettre en œuvre une hiérarchie d'horloge. Cette hiérarchie comprend (fig. 3-13) une horloge globale distribuée par une grille, six horloges principales (grilles également) et des horloges locales conditionnelles (localement, ces horloges peuvent être inhibées). L'horloge globale est routée sur les niveaux de métallisation les plus élevés et utilise 3% de la ressource.

3.4.2 Microprocesseur G5 S/390 IBM

Ce microprocesseur a été réalisé à l'origine avec une technologie 0,25 µm (1999). L'horloge comprend un arbre principal (L0, fig. 3-15), seize arbres secondaires (L1) et une grille locale. L'arbre principal est routé sur les deux premiers niveaux de métallisation, ses lignes sont protégées par des lignes d'alimentation. A l'extrémité de chaque branche de l'arbre principal, un *buffer* alimente un arbre secondaire, qui, à son tour, alimente une grille de 32 lignes et 32 colonnes.

3.4.3 Microprocesseur Intel IA-64

L'IA-64 est le premier microprocesseur 64-bits d'Intel. Le cœur comprend 25,4 millions de transistors et mesure 464 mm^2. Il est fabriqué en technologie 0,18 µm (2000) et travaille à 800 MHz. La structure de distribution d'horloge (fig. 3-17) comprend un niveau global (arbre en H routé sur les deux niveaux de métallisation les plus élevés), un niveau régional (une grille qui occupe environ 4% des niveaux de métallisation 4 et 5) et un niveau local.

3.5 *Evolution des systèmes de distribution d'horloge*

A mesure que la technologie progresse, il est de plus en plus difficile de transmettre un signal d'horloge dont les transitions sont parfaitement déterminées et abruptes. De plus, le *skew* est lui même de moins en moins contrôlable et il est irréaliste de vouloir transmettre une horloge à quelques gigahertz sur la surface entière d'un circuit.
Une des solutions pour relaxer ces contraintes est de distribuer l'horloge à deux fréquences différentes: une horloge globale diffuse un signal de fréquence relativement faible sur toute la surface du circuit et des horloges locales rapides, obtenues à partir de l'horloge lente par multiplication de fréquence, synchronisent une partie seulement du circuit (La figure 3-19 montre les prévisions de l'ITRS concernant les fréquences des horloges globale et locale pour les générations technologiques successives). Cette solution conduit à des

architectures dites GALS (***g****lobally* ***a****synchronous and* ***l****ocally* ***s****ynchronous*) [CHA-84, HEM-99, MEI-99, MUT-00, SJO-00]: le circuit est divisé en modules synchrones qui communiquent entre eux de manière asynchrone.

3.6 *Conclusion*

Ce chapitre a passé en revue les techniques mises en œuvre pour distribuer l'horloge dans les circuits complexes. Il a décrit les principales contraintes de conception des réseaux de distribution d'horloge et, en particulier, le *skew*. Enfin, un certain nombre d'exemples réels ont été présentés.

Chapitre IV

Modélisation du réseau de distribution d'horloge électrique

4.1 *Introduction*

A cause de la réduction constante du paramètre technologique, de l'augmentation corrélative des fréquences de travail et la complexité des circuits, le rôle des interconnexions dans les performances des circuits croît. Cette évolution conduit à ce que les interconnexions jouent un rôle toujours plus grand dans la conception d'un circuit [RAH-95, HOR-99, SAK-00, YAM-00, DAV-01]. Les simulateurs doivent donc ....

4.2 *L'estimateur de performances ICAL*

Ce chapitre décrit l'outil appelé ICAL (***I****nterconnect* ***Cal****culator*) permettant de modéliser puis de simuler un réseau de distribution d'horloge. Ce programme permet de prédire et d'optimiser les RDH pour les générations technologiques futures. Les données d'entrées par défaut sont extraites de la *roadmap* de l'ITRS. L'architecture du réseau et la structure des interconnexions sont prises en compte. Le coeur du calculateur s'appuie sur des modèles analytiques extraits de la littérature publiée sur le sujet.
L'organigramme de ICAL est donné par la figure 4.2, les paramètres d'entrée sont les paramètres technologiques donnés par l'ITRS. ICAL calcule alors les paramètres électriques des interconnexions (résistance, capacité et inductance linéiques) et des transistors. ICAL optimise ensuite le nombre et la taille des répéteurs du réseau. Il génère ensuite la *netlist* Spice du réseau. Les performances temporelles du réseau et sa consommation de puissance sont enfin déterminées soit analytiquement, soit à partir des résultats de simulation Spice.

4.3 *L'unité de modélisation des interconnexions*

Ce paragraphe présente les modèles utilisés dans ICAL pour simuler la propagation sur les lignes d'interconnexion.

4.3.1 Résistance

La résistance linéique des interconnexions est déterminée par $R_0 = \frac{\rho}{W.T}$;

Où est la résistivité du matériau, W, la largeur de la piste métallique et T son épaisseur. Dans cette expression, les dimensions de la piste conductrice doive prendre en compte l'effet de peau (en effet, dans des pistes de cuivre, la profondeur de peau est de 2µm à 1GHz).

4.3.2 Capacité linéique

L'estimation de la capacité linéique des lignes d'interconnexions pour des technologies fortement submicroniques n'est pas tâche aisée et a conduit à de nombreuses études [RUE-75, BER-88, LEE-98]. En particulier, il est essentiel de disposer d'un modèle précis pour le calcul de la capacité de recouvrement entre conducteurs. Cependant, il est bien sûr inenvisageable d'utiliser des simulateurs bi- ou tridimensionnels

[JEN-94, CHE-96] pour calculer la capacité linéique, aussi, de nombreux modèles analytiques ont-ils été proposés.

L'équation la plus simple pour déterminer la capacité s'écrit $C = \varepsilon_0 \varepsilon_{SiO_2} \frac{W}{H} L_{int}$; H est l'épaisseur de la couche diélectrique séparant les couches métalliques (ILD: *interlayer dielectric*), W est la largeur de la ligne et L_{int} sa longueur.

La plus grande part de la capacité d'un lien provient en fait du couplage entre les lignes adjacentes routée sur la même couche de métal et entre des lignes situées sur des couches métalliques adjacentes (fig. 4-5): le modèle de capacité plane est inutilisable.

De nombreux modèles analytiques ont été publiés [SAR-82, SAK-83, CHER-92, WON-00]. Nous avons comparé les résultats de ces modèles et les résultats obtenus grâce au logiciel commercial Opera [VEC] qui utilise une méthode d'éléments finis pour résoudre les équations de Maxwell. Cette comparaison a porté sur des structures d'interconnexions pour des technologies 130, 100 et 50 nanomètres.

La formule de Chern (équation 4-11) présente une erreur relative inférieure à 8% vis à vis des simulations électromagnétiques, pour une large gamme de paramètres des interconnexions. C'est cette équation empirique qui a été intégrée dans ICAL.

4.3.3 Inductance

A cause de l'augmentation des fréquences de fonctionnement, de celle des longueurs des interconnexions et de la réduction de la résistance des lignes, les phénomènes inductifs ne peuvent plus être négligés dans les circuits actuels [DEU-95, DEU-97, KRA-98, ISM-99, ISM-00]. Ces phénomènes ont des effets significatifs sur le temps de propagation, l'intégrité des signaux (à cause d'éventuels comportements pseudopériodiques) et les interférences entre pistes voisines.
La difficulté principale dans l'estimation de l'inductance des lignes tient au fait qu'elle est fonction de l'aire de boucles de courant fermées et qu'il est en général difficile de déterminer avec précision les chemins de retour. ICAL intègre des expressions analytiques approchées pour l'estimation de l'inductance et la mutuelle inductance de lignes à section rectangulaire [GRO-45].

4.3.4 Modèles électriques des interconnexions

A l'origine les interconnexions ont été modélisées par des circuits R-C à constantes localisées [RUB-83]. L'augmentation des fréquences de fonctionnement des circuits et donc de la réduction des longueurs d'onde des signaux se propageant, a conduit à l'utilisation de modèles à constantes réparties (fig. 4.11).

L'équation de propagation pour un modèle à constantes réparties R-C s'écrit: $RC\frac{\partial V}{\partial t} = \frac{\partial^2 V}{\partial x^2}$.

Lorsque la longueur du lien est suffisamment longue pour que le temps de propagation devienne comparable avec le temps de montée des signaux et lorsque la résistance du lien est suffisamment faible pour ne pas annihiler les effets inductifs, un modèle à constantes réparties R-L-C doit être utilisé.

L'équation de propagation devient alors: $\frac{\partial^2 V}{\partial x^2} = RC\frac{\partial V}{\partial t} + LC\frac{\partial^2 V}{\partial t^2}$.

ICAL intègre ces modèles à constantes réparties (par défaut, ICAL utilise un modèle R-L-C).

4.3.5 Modèle électrique équivalent d'un arbre en H symétrique

ICAL génère une *netlist* Spice pour simuler le temps de propagation du signal dans les branches de l'arbre de distribution. La précision de la simulation des interconnexions impose que le nombre de cellules R-L-C modélisant une branche soit élevé (supérieur à quelques dizaine), aussi le nombre de nœuds de la *netlist* conduit à des temps de simulation prohibitifs.

Un modèle électrique équivalent de l'arbre (fig. 4-14) permet de réduire le nombre de nœuds nécessaire à sa simulation.

4.4 *Modélisation des composants actifs*

L'arbre de distribution d'horloge comprend des *buffers* qui, d'une part, remettent le signal en forme et, d'autre part, permettent de réduire la dépendance du temps de propagation avec la longueur de la ligne. Un segment d'interconnexion est constitué d'un inverseur CMOS pilotant un autre inverseur à travers une ligne de propagation (fig. 4-15-a).
Dans ICAL, les inverseurs sont modélisés par le schéma équivalent de la figure 4-16-a (D_v représente le retard interne de l'inverseur, R_{inv} la résistance de sortie, C_{in} la capacité d'entrée et V est l'excursion de tension) ou par le schéma à transistor de la figure 4-16-b qui utilise les modèles BSIM3 et BSIM4.

4.4.1 Résistance de sortie des inverseurs

La résistance de sortie d'un transistor peut être approximée par la somme de la résistance de canal et des résistances d'accès à la source et au drain: $R_{tr} = R_{ch} + 2.R_c$.

La résistance de canal peut être calculée par $R_{ch} = \frac{L_t / W_t}{\mu C_{ox}(V_{DD} - V_T)}$ [VEE-00]. La résistance d'accès à la source et au drain est donnée par $R_c = \frac{\rho_c}{A_{contact}}$; expression dans laquelle ρ_c représente la résistivité du matériau assurant le contact et $A_{contact}$ est la surface du contact de source ou de drain.

La résistance de sortie de l'inverseur dépend des résistances des transistors NMOS et CMOS constituant l'inverseur.

4.4.2 Capacités d'entrée et de sortie de l'inverseur

La figure 4-18 décrit les différents éléments capacitifs d'une structure MOS.
Ces différentes composantes capacitives peuvent être calculées analytiquement à partir des paramètres technologiques des générations successives et permettent de calculer les capacités d'entrée et de sortie de l'inverseur.

4.5 *Optimisation*

Ce paragraphe présente la méthode d'optimisation implantée dans ICAL, elle est fondée sur l'expression analytique du temps de retard sur une ligne d'interconnexion.

4.5.1 Expression du retard dans une ligne R-C

La modélisation du temps de propagation d'un signal délivré par une porte CMOS sur une charge capacitive a fait l'objet de nombreuses études [ELM-48, SAK-93, DEN-90].
Le circuit équivalent de la figure 4-22 permet de déterminer le temps de propagation (R_{buf} est la résistance de sortie de la porte CMOS d'entrée, R_{int} et C_{int} sont les résistance et capacité linéiques de l'interconnexion et C_{buf} est la capacité de sortie de la porte de réception.
ICAL utilise la formule de Sakurai [SAK-93]:

$$T_v = 0{,}1R_{int}C_{int} + \mathrm{Ln}\left(\frac{1}{1-v}\right)\left(R_{buf}C_{int} + R_{int}C_{buf} + R_{buf}C_{buf} + 0{,}4R_{int}C_{int}\right);$$

$T_{\square}$ représente le temps de retard nécessaire pour que le signal de sortie atteigne la tension $V=\square V_{DD}$.

4.5.2 Insertion de répéteurs

L'utilisation de répéteurs pour diviser l'interconnexion en segments de dimension plus réduite permet de réduire le temps de propagation. La méthode proposée par Bakoglu [BAK-85] permet de réduire la dépendance du temps de propagation en fonction de la longueur de la ligne d'une dépendance quadratique à une dépendance linéaire.

La figure 4-23 représente une ligne de longueur l, divisée en K segments, chacun de ces segments étant alimentés par un *buffer*.
La formule de Sakurai, dans cette configuration prend alors l'expression suivante:

$$T_{delay} = \frac{0,377R_{int}C_{int}}{K} + 0,693\left(R_{buf}C_{int} + R_{int}C_{buf} + K.R_{buf}C_{buf}\right).$$

Par ailleurs, la résistance interne et la capacité d'entrée des répéteurs dépendent de leur taille. Il est donc possible de minimiser le délai de propagation en optimisant la taille des répéteurs.
Si R_0 et C_0 sont la résistance de sortie et la capacité d'entrée d'un inverseur élémentaire, la résistance de sortie et la capacité d'entrée d'un répéteur h fois plus grand sont égales à R_0/h et $h.C_0$.

Le délai de propagation prend alors la forme suivante:

$$T_{delay} = \frac{0,377R_{int}C_{int}}{K} + 0,693\left(\frac{R_0C_{int}}{h} + R_{int}C_0h + K.R_{buf}C_{buf}\right).$$

La minimisation de T_{delay} conduit aux valeurs optimales de K et de h: $K_{opt} = \sqrt{\frac{0,377R_{int}C_{int}}{0,693R_0C_0}}$ et $h_{opt} = \sqrt{\frac{R_0C_{int}}{R_{int}C_0}}$.

4.5.3 Expression du retard dans une ligne R-L-C

Les relations précédentes, pourtant largement utilisées, ne peuvent prendre en compte les phénomènes inductifs qui causent des oscillations et des surtensions. Ical utilise le formalisme de Ismail et Friedman [ISM-00] qui exprime le retard de propagation pour tous les régimes d'amortissement d'une ligne R-L-C.

Le temps de retard à 50% (fig. 4-24) est exprimé par: $T_{RLC}^{50\%} = \left[\exp\left(-2,9\zeta^{1,35}\right) + 1,48\zeta\right]\omega_n$,

où ω_n représente la pulsation caractéristique : $\omega_n = \frac{1}{\sqrt{L_{int}\left(C_{int} + C_{Load}\right)}}$

et ζ, le facteur d'amortissement: $\zeta = \frac{R_{int}}{2}\sqrt{\frac{C_{int}}{L_{int}}}\frac{R_{tr} + C_{Load} + R_{tr}C_{Load} + 0,5}{\sqrt{1 + C_{Load}}}$.

4.5.4 Insertion de répéteurs

Une méthode d'optimisation du nombre et de la taille des répéteurs nécessaires pour minimiser le temps de retard analogue à la méthode utilisée dans le cas des lignes R-C a été développée [ISM-98, ISM-99b, ISM-00, ISM-01], Ical intègre ces résultats:

Le nombre optimal de répéteurs s'exprime par $K_{opt}^{RLC} = \sqrt{\frac{R_{int}C_{int}}{2R_0C_0}}\frac{1}{\left[1 + 0,18\left(T_{L/R}\right)^3\right]^{0,3}}$, leur surface est égale à $S_{opt}^{RLC} = \sqrt{\frac{R_0C_{int}}{R_{int}C_0}}\frac{1}{\left[1 + 0,16\left(T_{L/R}\right)^3\right]^{0,24}}$, expressions dans lesquelles $T_{L/R} = \sqrt{\frac{L_{int}/R_{int}}{R_0C_0}}$.

4.5.5 Cascade de répéteurs

Ical intègre également une méthode d'optimisation des *buffers*. En effet, pour piloter de fortes charges, la taille des transistors constituant les répéteurs est élevée. Il est possible de minimiser le temps de retard dû aux répéteurs en associant une cascade d'inverseurs (fig. 4-25). Chaque inverseur a une taille f fois supérieure à celui qui le précède, le temps de retard dans ce répéteur s'écrit alors:

$$T_{delay} = 0{,}377 R_{int} C_{int} + 0{,}693\left(\frac{R_0}{f^{N-1}} C_{int} + (N-1) f R_0 C_0 + R_{int} C_0 \right).$$

La minimisation du temps de retard dans les répéteurs conduit au résultat classique: f=e≅2,72.

4.6 *Conclusion*

Le chapitre 4 a présenté l'outil Ical développé durant cette thèse. Il permet de modéliser, optimiser et évaluer les performances les réseaux de distribution d'horloge. Ical permet en particulier d'optimiser le nombre et la taille des répéteurs. Une *netlist* Spice est extraite de Ical, ce qui permet de simuler le comportement temporel du réseau et de déterminer la puissance qu'il consomme.

Chapitre V

Interconnexions optiques

5.1 *Introduction*

Le concept d'interconnexion optique est une solution potentielle attractive qui pourrait permettre de résoudre la plupart des problèmes posés par les interconnexions globales *on-chip*. Leurs avantages couramment cités sont une capacité de transmission énorme, l'absence de phénomènes d'interférences électromagnétiques, une grande densité d'interconnexion et une faible consommation de puissance.
De nombreux travaux ont été menés récemment [WU-87, FAN-95, LEV-00, CRI-01, HIM-01] qui visent à utiliser l'optique pour la réalisation de liens *on-chip*; la difficulté majeure réside dans l'intégration, sur la même puce, de composants optiques et électriques, ce qui soulève des problèmes technologiques ardus.
Du point de vue élémentaire, les phénomènes de propagation des signaux électriques et optiques sont très similaires [MIL-96]: dans les deux cas le signal est porté par une onde électromagnétique. La figure 5-1 met en évidence les principales différences: l'onde optique est caractérisée par une longueur d'onde plus faible (et donc une fréquence plus élevée) et une énergie des porteurs plus élevée.
Pour profiter pleinement des avantages de l'optique dans la réalisation de liens *on-chip*, de nombreuses avancées technologiques doivent être faites pour intégrer sur un circuit VLSI standard des émetteurs et des récepteurs optiques et des canaux de transmission.

5.2 *Récepteurs optiques*

5.2.1 Structure générale d'un récepteur

Le récepteur est le composant le plus critique d'un lien optique. Son rôle est de convertir le signal optique en signal électrique, en minimisant le bruit et la distorsion. Le récepteur peut en général être séparé en trois blocs (fig. 5-3), le signal optique est converti par le photodétecteur puis un préamplificateur délivre une tension de faible amplitude en minimisant le bruit, un deuxième étage d'amplification permet de délivrer une tension d'amplitude plus élevée et un circuit de décision génère le signal numérique.

5.2.2 Photodiodes

Les détecteurs peuvent être des photodiodes ou des phototransistors. Les photodiodes sont adaptées aux applications à haute fréquence du fait de leur meilleure réponse fréquentielle. Les paramètres principaux permettant de sélectionner un détecteur sont sa longueur d'onde de fonctionnement, sa vitesse et sa sensibilité.
Un jonction PN polarisée en inverse est la photodiode la plus simple. Une structure PIN permet d'améliorer la sensibilité du détecteur. Pour des applications à haute fréquence, c'est la structure la plus adaptée.

5.2.3 Préamplificateurs

Le préamplificateur joue un rôle fondamental dans les performances globales du lien. Son rôle est de convertir le photocourant en une tension de faible amplitude. La principale difficulté dans la conception porte sur le compromis bande passante/ sensibilité.

Trois solutions principales peuvent être identifiées : la topologie à amplification de tension (fig. 5-5) ou l'amplification transimpédance (fig. 5-6).

Lorsque la résistance de conversion est relativement faible (environ 50□), il est possible d'atteindre des bandes passantes importantes au prix d'une sensibilité réduite et de la génération d'un important bruit thermique. Une résistance R_B plus élevée améliore la sensibilité et le comportement en bruit au détriment de la bande passante.

Le montage transimpédance est le plus largement utilisé dans les applications à haute vitesse : il sera retenu dans les analyses suivantes.

Dans le but de déterminer la puissance optique minimale acceptable, il est nécessaire de conduire une analyse du rapport signal à bruit à la sortie du photorecepteur.
D'après Morikuni, la fonction de transfert de l'étage transimpédance peut être exprimée par l'équation 5-2 et la densité spectrale de puissance du bruit généré par la photodiode et l'amplificateur transimpédance peut être exprimée par l'équation 5-8.

5.3 *Sources optiques*

5.3.1 Lasers à semiconducteur

Le rôle des sources est de convertir le signal électrique en signal optique. Les sources possibles sont les diodes électroluminescentes (LED) et les lasers à semiconducteur. Pour des raisons touchant à leurs performances en termes de divergence du faisceau, de bande passante accessible et de largeur spectrale, les LED ne sont pas adaptées aux communications à haute vitesse.
Il existe deux grands types de lasers : les lasers émettant par la tranche (qui dominent le marché des communications à longue distance) et les lasers émettant par la surface (VCSEL : *vertical cavity surface emitting laser*).
Du fait de la taille réduite de leur cavité (conduisant à des courants de seuil potentiellement faibles) et de leur procédé collectif de fabrication, les VCSELs sont les candidats les plus sérieux pour des communications à courte distance.

5.3.2 Circuits de commande

Le circuit de commande doit assurer la polarisation du laser (afin d'en optimiser le comportement dynamique) et moduler la puissance optique au rythme du signal à transmettre. Deux exemples de circuits de commande simples [KRI-99, MAT-97] sont présentés par la figure 5-9.

5.4 *Composants passifs*

Les guides d'onde optiques permettent de guider la lumière, ils sont constitués de deux matériaux diélectriques : un matériau d'indice élevé (le cœur) est entouré d'un matériau d'indice plus faible (la gaine). La lumière est guidée dans le cœur.

5.4.1 Fibres optiques

Les fibres sont des guides cylindriques. En fonction du diamètre du cœur (et des indices du cœur et de la gaine), on distingue des fibres monomodes et multimodes.

5.4.2 Guides planaires semi-infinis

Ces guides (fig.5-12) sont des structures bidimensionnelles pour lesquelles il est possible de résoudre analytiquement les équations de Maxwell. La lumière est confinée dans la couche à fort indice, la constante de propagation peut être calculée (eq.5-10) ainsi que les conditions géométriques d'une propagation monomodale (eq. 5-18).

5.4.3 Guides planaires

Les guides réels utilisés en optique intégrée ont une section finie (fig. 5-14). Le comportement de la propagation de la lumière dans ce type de structure ne peut être déterminé de façon simple, des méthodes approchées permettent néanmoins de prévoir le comportement de ces structures.

Dans notre analyse, nous avons utilisé le guide de la figure 5-14-a, il a été réalisé en technologie SOI (le cœur est constitué de silicium, n~3,5, et la gaine de silice, n~1,5). Le fort contraste d'indice entre les deux matériaux permet de réaliser des structures compactes compatibles avec les contraintes d'encombrement des circuits intégrés.

5.5 *Conclusion*

Chapitre VI

Réseau optique de distribution d'horloge

6.1 *Introduction*

Les interconnexions optiques peuvent résoudre la plupart des limitations des technologies classiques, en effet, elles sont susceptibles de procurer de grandes bandes passantes et de permettre la réduction de la puissance consommée et des interférences entre signaux (*crosstalk*).
Récemment de nombreuses voies ont été explorées pour transmettre une horloge par voie optique : on peut distinguer trois grandes approches.
La figure 6-1 présente une distribution non confinée : une source externe diffuse un signal optique à un ensemble de récepteurs répartis sur le circuit ; cette approche souffre d'un rendement faible puisque une faible part de la puissance optique est effectivement utilisée pour la transmission.
Les figures 6-2-a et 6-2-b montrent deux exemples de systèmes confinés. Dans le premier, le signal optique est confiné dans le plan de propagation grâce à des éléments réfractifs ou des miroirs [WAL-92, TAN-94, YEH-95, ZHA-97, lun-97]. Dans le second, un hologramme permet de concentrer le signal optique vers les récepteurs [BRE-88, HAU-91, MOR-00, NAK-02].
Enfin, la figure 6-3 présente une distribution guidée. Cette solution a été largement étudiée ces dernières années [DEL-91, KOH-94, GIO-98, LI-99, MUL-00, SAM-01, FUK-02].

6.2 *Architecture proposée*

Dans le but de comparer, sans ambiguïté, leurs performances, nous avons construit un réseau optique de distribution d'horloge équivalent au réseau électrique décrit au chapitre 2. Un VCSEL est couplé à un arbre symétrique passif et distribue le signal optique à n photorécepteurs (fig.6-4), le signal optique est alors converti et distribué aux bascules par des arbres secondaires électriques.
La figure 6-5 montre un arbre à 64 nœuds de sortie, pour réduire la longueur des guides et minimiser les pertes de courbure, les rayons de courbure des différents tronçons sont les plus grands possibles.
Les guides sont fabriqués en SOI (fig. 6-6), ce qui permet d'assurer une technologie de fabrication compatible avec celle des circuits CMOS. Par ailleurs, les guides sont conçus pour être monomodes.

6.3 *Détermination des paramètres du réseau optique*

Les performances du réseau dépendent des paramètres de chaque composant le constituant. Les paragraphes suivants les décrivent plus précisément.

6.3.1 Taux d'erreur par bit

Le taux d'erreur par bit (TEB ou BER –*bit error rate*-) permet de mesurer la qualité globale du système. Il est possible de relier le TEB au rapport signal à bruit à la détection (fig. 6.8), ainsi, pout un TEB fixé il sera possible de déterminer la puissance optique nécessaire à la réception.

6.3.2 Puissance optique minimale

Le rapport signal à bruit permet de calculer la puissance optique minimale à la réception. Dans le cas général, il est possible d'exprimer cette puissance en fonction du facteur d'extinction (exprimé comme le rapport des puissances optiques des niveaux logiques « 0 » et « 1 ») : eq. 6-11.

A partir de P_{AVG}, en tenant compte des pertes dans le réseau de transmission, il est donc possible de déterminer la puissance que le VCSEL doit émettre pour assurer un TEB donné.

6.3.3 Pertes dans les composants passifs

Les pertes dans le réseau sont la somme des pertes de couplage à l'émission (L_{CV}), des pertes de transmission dans les guides (L_W), des pertes supplémentaires dues aux courbures (L_B), des pertes dans les jonctions en Y qui divisent le faisceau et des pertes de couplage à la réception (L_{CR}), eq.6-12.

6.3.3.1 Pertes dans les guides

Les pertes dans les guides sont dues à l'absorption due au matériau, à la diffusion et aux imperfections du guide.
En particulier, les imperfections des procédés de fabrication conduisent à ce que les flancs des guides exhibent une certaine rugosité (fig. 6-10). Ces pertes sont les plus importantes dans le système que nous simulons.
Les pertes peuvent être reliées à la rugosité des flancs (fig. 6-12).
Les meilleurs résultats publiés concernant les pertes dans des guides Si/SiO_2 sont de 0,8 dB/cm [LEE-01].

6.3.3.2 Pertes dues aux courbures

Dans le cas du système Si/SiO_2 , les pertes par courbure ne deviennent appréciables que pour des rayons de courbure inférieurs à quelques microns. La conception de l'arbre de distribution rend ces pertes négligeables.

6.3.3.3 Pertes des jonctions en Y

Les jonctions en Y permettent de diviser la puissance optique afin de la distribuer sur le circuit. Différentes structures ont été proposées [SAK-02], (fig.6-15), la structure adoptée (fig.6-15-f) apporte un excès de perte de 0,1dB.

6.3.3.4 Pertes de couplage

Un paramètre essentiel dans les systèmes de transmission est celui du couplage entre le milieu de transmission et l'émetteur et le récepteur.
Nous avons supposé que la source optique était externe dans notre système. Dans l'état actuel de la technologie plusieurs méthodes ont été utilisées pour coupler un laser avec un guide plan [KAR-90, GAN-98, MAR-88], fig.6-16. Ces méthodes de couplage direct nécessitent un *packaging* spécifique.
Le couplage par réseau ou par miroir nous emble préférable (fig.6-17), et certains auteurs rapportent des coefficient de couplage proches de 100% [SCH-98, SCH-00, MUL-01].

6.4 *Conclusion*

Ce chapitre a permis de décrire le réseau de distribution que nous avons comparé à un réseau électrique classique. Les paramètres essentiels des différents composants élémentaires ont également été présentés.

Chapitre VII

Comparaison des réseaux électrique et optique

7.1 *Introduction*

Les interconnexions optiques apparaissent comme une solution susceptible de résoudre une partie des problèmes posés par les interconnexions métalliques. Cependant, il est nécessaire de montrer que le surcoût technologique de cette solution peut être compensé par un net gain de performances.
C'est dans cette perspective que nous proposons dans ce chapitre une comparaison fiable des performances en termes de puissances consommées, pour les technologies futures.

7.2 *Distribution électrique*

Ical permet de calculer la consommation de puissance dans un arbre conventionnel. Le jeu initial de paramètres nécessaire à Ical est extrait de l'ITRS (tableau 7-1). A partir de ces paramètres Ical détermine les constantes réparties caractéristiques des lignes métalliques. Puis, en utilisant les paramètres prévisionnels des transistors représentatifs des nœuds technologiques futurs [BSIM], Ical détermine le nombre et la taille des *buffers* nécessaires pour respecter les contraintes temporelles imposées par la fréquence de l'horloge. Enfin, Ical permet de calculer la consommation de puissance dans les différents éléments de l'arbre d'horloge.

La figure 7-1 donne, pour les nœuds technologiques successifs, la taille des *buffers* et la longueur des segments de lignes optimales (un modèle RLC des lignes est utilisé, cf. chap.IV).
La figure 7-2 donne le nombre de transistors utilisé dans l'arbre et la surface qu'ils occupent. On constate que, comme il était prévisible, le nombre de transistors utilisés dans les *buffers* augmente considérablement alors que la surface qu'ils utilisent reste constante.
Enfin, les figures 7-3 et 7-4 mettent en évidence l'évolution dans le temps de la consommation de puissance de l'arbre électrique.

7.3 *Distribution optique*

L'architecture générale de l'arbre de distribution optique a été présentée dans le chapitre précédent. Le tableau 7-3 précise les paramètres du système optique.
Les deux sources principales de dissipation sont, d'une part les amplificateurs et d'autre part la puissance délivrée à la source optique : le schéma synoptique de la figure 7-5 résume le flot de calcul qui permet d'estimer la puissance totale dissipée dans l'arbre de distribution.
Tout d'abord, l'amplificateur transimpédance est conçu à partir des paramètres de la photodiode (en particulier de sa sensibilité et de sa capacité de jonction) et des contraintes de bande passante. Ensuite, pour un TEB donné, la puissance optique minimale que doit recevoir chaque phtodétecteur est calculée. Enfin, en tenant compte des pertes du circuit passif, la puissance dissipée dans le VCSEL est déterminée.

Les figures 7-7 à 7-12 présentent un certain nombre de résultats d'estimation de la puissance consommée dans l'arbre optique en fonction des paramètres macroscopiques du système (en particulier, du nombre de nœuds dans le réseau optique et du TEB choisi).

7.4 *Comparaison des arbres électrique et optique*

Ce paragraphe présente une synthèse des principaux résultats de comparaison de la consommation de puissance des arbres de distribution électrique et optique.
La figure 7-13 permet de comparer la puissance consommée en fonction de la fréquence de l'horloge, ces résultats sont établis pour une technologie 70nm.
La figure 7-15 montre l'impact du nombre de nœuds de l'arbre ; enfin, la figure 7-17 met en évidence l'évolution des puissances dissipées en fonction du nœud technologique.

7.5 *Conclusion*

Ce chapitre a présenté les principaux résultats de l'estimation des puissances consommées par des arbres de distribution électrique et optique pour les futurs nœuds technologiques.

Chapitre VIII

Conclusions

Dans cette étude, l'alternative optique aux limitations imposées par les interconnexions métalliques a été analysée. Puisque le réseau de distribution de l'horloge prend une part essentielle à la consommation globale d'un circuit intégré, la distribution d'horloge a servi de système de test.

La puissance consommée par un réseau métallique a été calculée et des projections ont pu être faites pour les nœuds technologiques futurs : l'estimateur de performances Ical permet en effet de déterminer la puissance consommée dans les lignes métalliques ainsi que dans les *buffers* répartis sur l'arbre d'horloge.
De manière analogue, la puissance totale consommée dans un arbre de distribution optique a été estimée, le calcul prend en compte la puissance consommée dans la source optique, dans le réseau de distribution proprement dit et dans les photorécepteurs.

Ainsi, une comparaison fiable des deux technologies a pu être proposée. Elle montre que la puissance dissipée dans l'arbre primaire optique peut être jusqu'à 5 fois inférieure à la puissance consommée dans le réseau classique.

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ζ	Damping factor
η	Detector quantum efficiency
$\Re$	Photodiode responsivity
β	Propagation constant
ρ	Resistivity of the metal layer
δ	Skin depth
λ	Wavelength
μ_o	Magnetic permeability
ε_o	Permittivity of free space
$A_{contact}$	Area of the contact window
A_{Int}	Cross-section area of the conductor
$C_{bottom\text{-}plate}$	Transistor bottom-plate junction capacitance
C_F	Fringing field capacitance component
C_{gate}	Gate capacitance
C_{IN}^{inv}	Input capacitance of minimum size inverter
C_L	Lateral coupling capacitance component,
C_o	Interconnect capacitance per unit length
C_{OUT}^{inv}	Output capacitance of minimum size inverter
C_{ox}	Oxide capacitance
C_P	Parallel plate capacitance component
$C_{side\text{-}wall}$	Transistor side-wall junction capacitance
erfc	Error function
f	Optimal tapered factor
g_m	Transconductance
H	Interlayer dielectric thickness
h_{Opt}	Optimal buffer size
I_{dark}	Photodiode dark current
I_{gate}	Transistor gate current
$I_{leakage}$	Leakage current
I_{sat}	Saturation current

I_{sc}	Short-circuit current
k	Boltzmann's constant
k_o	Free-space wavenumber
K_{Opt}	Optimal buffer number
L_B	Bending loss
L_{CR}	Output coupling loss from the waveguide to the optical receiver
L_{CV}	Input coupling loss between the photonic source and optical waveguide
L_{Int}	Interconnection length
L_o	Interconnect inductance per unit length
L_t	Transistor channel length
L_W	Rectangular waveguide transmission loss
L_Y	Y-spliter loss
N	Optimal number of stages in tapered buffer
n_{eff}	Waveguide effective refractive index
p	Rent's exponent,
P_{AVG}	Average optical power needed by photodetector
$P_{dynamic}$	Dynamic power
$P_{leakage}$	Leakage power
$P_{short\text{-}circuit}$	Short-circuit power
q	Electron charge constant
R_c	Contact resistance
R_{Ch}	Transistor channel resistance
r_e	Extinction ratio
R_o	Interconnect resistance per unit length
S	Interconnect space
S	Technology scaling factor
T	Interconnect thickness
T_{ox}	Equivalent oxide thickness
T_{Skew}	Clock skew
U	Voltage scalling factor
V	Normalized waveguide frequency
v	Optical frequency
V_{DD}	Supply voltage
V_T	Threshold voltage
W	Interconnect width
W_t	Transistor channel width
Γ	Excess channel-noise factor

I. Introduction

Chapter I
Introduction

1.1 MOTIVATION.

Advances in semiconductor fabrication, have made it possible to design and fabricate chips with several millions of transistors operating at very high speeds. These advances are dynamically incorporated with innovative hardware organisations of modern integrated circuits (IC's) and achieve remarkably high performance at low cost. If the development of integrated circuits continues to increase its complexity at the same pace as since 1960, it will reach one billion transistors per chip within a decade from now. It becomes evident that most of the known technological capabilities will approach or have reached their fundamental limits. In order to realize gigascale integration (GSI) a variety of technological and architectural barriers must be overcome. In 1994 the Semiconductor Industry Association (SIA) published a technology roadmap of semiconductors [ITRS-94] in which the progress of IC's was predicted until the year 2010. In 1997 the roadmap was revisited [ITRS-97] and in April of 1998, at the World Semiconductor Council, the SIA invited several association from all regions of the world to cooperate on the *International Technology Roadmap for Semiconductors* (ITRS). As a result, two editions of ITRS roadmaps were launched in 1999 and 2001. If the ITRS gives a correct prediction of the next 15 years, progress in integrated circuits will remain the same as it has been for the past 30–40 years. However, many practical and fundamental limits are being approached and substantial changes in device technologies and structures will be required.

Progress of VLSI systems has been driven by the downsizing of its components and increasing of operating speed. While transistor scaling provides improvements in both density and device performance, interconnect scaling improves interconnect density but

generally at the cost of degraded propagation delay and power consumption. In new technologies, the interconnect delay dominates over logic delay, in spite even when new metallization technologies such as copper or new low-k dielectrics are applied. The introduction of new materials helps to increase the speed of interconnects by reducing resistance and capacitance per unit length. However these solutions also have penalties and only partially solve the interconnection problem.

In new VLSI chips, the downsizing of processes leads to smaller transistors supplied by smaller voltages and characterized by smaller power consumption, but the number of transistors and its density increases to such a degree that the resulting density of power dissipation increases. The simultaneous growth in circuit complexity leads to increasingly large chip dimensions, resulting in the total length of interconnection lines being of the order of few kilometers, and giving considerable contributions to the total power dissipation. As a result, in modern VLSI systems, the power dissipation increases rapidly, especially in the interconnection part and in a VLSI circuit with power dissipation of 100W [KUR-01], only the clock tree uses at least 30% of this power and it may even reach 50% [GRO-98], [KAW-98], [BAI-98], [TAM-00]. Due to natural limits in thermal management, this is a real barrier to the further progress of modern VLSI systems and just now, it has happened that manufactures must lower their ratings simply due to thermal reasons.

It is evident that interconnect is becoming an increasingly crucial design issue for current and future generation of VLSI technologies and will required a real breakthrough [DAV-01]. The use o f optical interconnect is considered to be one alternative solution that could overcome the limitations of metallic ones. Optics provides many features such as large bandwidth, low power requirements, reduced crosstalk and better isolation than semiconductor electronics can provide. Application of optical interconnections to electronic chips have been the subject of many research at least 15 years [GOO-84], [WU-87], [KRI-96], [KRI-98], [MIL-00]. However, this alternative can be acceptable only if it demonstrates significantly improved performance over the electrical solution.

This work presents a quantitative analysis of the performance gains of using optical interconnections in a conventional silicon chip. It constitutes a part of a larger research project, in which a new optoelectronic VLSI (OP-VLSI) solution with a layout covering silicon waveguides formed on silicon chip is investigated. Since the clock distribution

network (CDN) is the most representative component of modern VLSI circuits, which consumes a huge part of delivered power, it has been chosen as the test network in the numerical investigations. This work aims at estimating whether the replacement of the electrical clock distribution network by its optical counterpart leads to a significant reduction in power consumption both in present ICs and predicted by the ITRS roadmap. The considered H-tree architecture for CDN design has been chosen for the numerical investigations as the most representative one for large clock distribution systems. The power consumption in both optical and electrical solutions of such an H-tree is chosen as the main comparison criterion. The hypothesis, to be validated that corresponds to this work program can be stated as follows:

The introduction of an optical clock distribution network instead of the electric one will reduce the power consumption in essential way.

1.2 THESIS OUTLINE.

This thesis is split into 4 main parts. The first part, Chapter 2 based on the ITRS roadmap presents and discusses current and future trends in device and interconnect technology. The impact of technology scaling on power consumption, propagation time and interconnect capacity is presented. It is shown that many practical and fundamental limits are being approached, and substantial changes to interconnect technologies will be required.

The second part focuses on electrical clock distribution network issues. Chapter 3 gives a literary overview of clock systems implemented within high-performance integrated circuits. In this chapter, the fundamental terminology and concepts needed to understand a synchronous systems are introduced. Today's common circuit strategies and topologies used to distribute the clock signal are also discussed. Based on this chapter, the tool called ICAL is presented in Chapter 4. This program provides designers with the capability to model, evaluate, predict and optimize global clock distribution networks for future technologies. The models and the assumptions used by ICAL to accurately estimate the interconnect and device parameters are presented. Based on the regularity of the H-tree structure ICAL creates the SPICE netlist where the interconnects are replaced by RC or

RLC distributed lines coupled by buffers designed as CMOS inverters. The power dissipated in the system can be extracted from transistor-level simulations or from the implemented analytical formulas.

The third part focus on the optical systems. Chapter 5 reviews the optical technology available for implementing the optical communication system. Since the optical interconnect can eliminate most of the problems associated with electrical clock distribution networks, a new optical H-tree clock distribution architecture, in which optical waveguides are used as the signal paths, is proposed in Chapter 6. In order for the H-tree network to be equivalent to the global electrical H-tree, the classical approach in describing an n-level electrical H-tree distribution is adopted. The methodology and the assumptions used to properly design the optical H-tree are presented.

The last part of the thesis, Chapter 7, examines the power consumption in both electrical and optical H-tree clock distribution systems ranging from the 130nm down to the 45nm technology node. In the case of electrical distribution, the power consumption takes into account the power dissipated in the buffers and by the interconnects of an optimized balanced H-tree. In the case of the optical clock distribution system, the calculations take into account the power dissipated in the optoelectronic conversion circuits; the power dissipated by the optical receivers and the energy needed by the optical source to provide the required optical output power. Electrical and optical system are compared in terms of dissipated power for the considered range of technology nodes.

II. Technology Trends

Chapter II

Technology Trends

2.1 INTRODUCTION.

The main objective of the ITRS, launched in 1999, is to ensure advancements in the performance of integrated circuits. The presented there history and predicted future of device scaling trend is presented in Fig.2.1. [PLU-01]. If it is correct, then during the next 15 years, progress in integrated circuits will continue at the same rate as that over the past 30–40 years. What means that many practical and fundamental limits are being approached and substantial changes to device technologies and structures will be required.

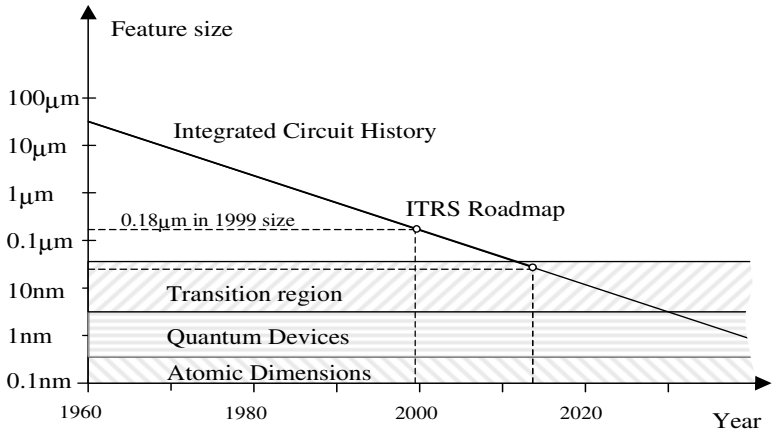


Fig.2.1. Feature size versus time in silicon IC's [PLU-01].

Progress of VLSI systems has been driven by the downsizing of its components and increasing operating speed. While transistor scaling provides improvements in both density and device performance, interconnect scaling improves interconnect density but generally

at the cost of degraded propagation delay and power losses. Based on ITRS technology predictions this chapter discusses the consequence of the scaling process for deep-submicron IC design.

2.2 DEVICE SCALING.

The continuing exponential reduction in feature sizes on electronic chips is known as Moore's law [MOO-65]. Just four years after the first planar integrated circuit was invented, Moore observed an exponential growth in the number of transistors per integrated circuit and predicted that this trend would continue. Moore noticed that the number of transistors per square inch on IC's had doubled every year since the integrated circuit was invented. In order to illustrate this Fig.2.2. shows the number of transistors in a single chip for Intel microprocessors as a function of time.

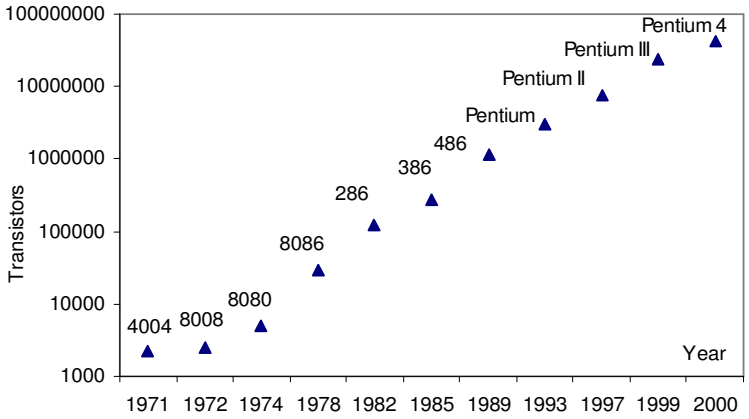


Fig.2.2. Evolution of number of transistor in IC's.

In subsequent years, the pace slowed down slightly, but data density has doubled approximately every 18 months, and this is the current definition of Moore's Law. The number of components on a chip grows annually with a factor according to Moore's law. On the other hand, the size of a chip has not significantly increased during the years. Chips have scaled from 2mm × 2mm in the early 1960s to approximately 2cm × 2cm in 2000.

The size of a typical die is increasing by 6% per year, doubling about every decade. This is because probability that the silicon wafer contains an undesired impurity or a mechanical flaw increases quickly with larger area.

A large part of the MOS IC's success is due to the fact that the scaling of the MOSFET transistor has been the primary factor driving improvements in microprocessor performance. The design of MOSFET's at progressively smaller dimensions has been consistent with the scaling criteria proposed by Dennard *et al.* [DEN-74] in the early 1970's. Dennard showed that to yield the smaller device, the larger device was scaled down by a factor *S*. In addition to the minimum device dimension, it is necessary to consider the supply voltage as a second independent scaling variable. All voltages, including supply voltages and the threshold voltages, are scaled by the same ratio *U*. Three different scaling scenario for short channel devices with linear dependence between control voltage and saturation current are presented in Table 2.1.

Table 2.1 *Scaling scenarios for short-channel devices.*

Parameter	Full Scaling	Fixed-Voltage Scaling	General Scaling
W_t, L_t, T_{ox}	$1/S$	$1/S$	$1/S$
V_{DD}, V_T	$1/S$	1	$1/U$
N_{SUB}	S	S^2	S^2/U^2
Device Area	$1/S^2$	$1/S^2$	$1/S^2$
C_{ox}	S	S	S
C_{gate}	$1/S$	$1/S$	$1/S$
I_{sat}	$1/S$	1	$1/U$
Current Density	S	S^2	S^2/U^2
R_{on}	1	1	1
Gate Delay	$1/S$	$1/S$	$1/S$
P	$1/S^2$	1	$1/U^2$
Power Density	1	S^2	S^2/U^2

The first ideal scaling scenario, called "Full Scaling", assumes that both voltages and dimensions are scaled by the same factor *S*. The second scenario, called "Fixed-Voltage

Scaling", assumes decreasing device dimensions, while the voltage keeping unchanged. And the last scenario, called "General Scaling", assumes that dimensions and voltage are scaled independently. The device dimensions are scaled by a factor *S*, while the voltages are reduced by a factor *U*. In order to illustrate the issue of device scaling, some of the most important device parameters predicted by ITRS 2002 technology roadmap are shown in Table 2.2.

Table 2.2. *The most important IC characteristics according to ITRS roadmap.*

Year of production	2003	2005	2007	2010	2013	2016
Minimum feature size [nm]	107	80	65	50	35	25
Equivalent oxide thickness [nm]	1.1-1.6	0.8-1.3	0.6-1.1	0.5-0.8	0.4-0.6	0.4-0.5
Supply voltage [V]	1	0.9	0.7	0.6	0.5	0.4
Transistor density [Mtr/cm^2]	26	47	85	210	519	1279
NMOS saturation current [μA/μm]	900	900	900	1200	1500	1500
Source/drain resistance [ohm-μm]	180	180	140	110	90	80
On-chip frequency [MHz]	3000	5170	6740	11511	17000	25000
Wafer size [mm^2]	300	300	300	450	450	450

Note that the physical channel length is expected to be 10–30% less than minimum feature size listed in Table 2.2, depending on the manufacturer. From the above, it is obvious that both integration density and systems performance will continue to increase. However, many practical and fundamental limits are being approached and substantial changes to device technologies and structures will be required.

2.3 INTERCONNECT SCALING

The performance of modern integrated circuits is often determined by interconnect wiring requirements. Moreover, continuous scaling of VLSI circuits leads to an increase in the influence of interconnect on system performance. For example, in the mid-1980's, devices having ~1μm feature sizes were in mass production, having typically one or two

layers of aluminum. Chips fabricated at the 0.25µm technology mode have six layers of copper interconnect, and according to ITRS prediction, chips will have eleven layers of metal at 0.035µm technology generation in 2011. In order to show the complexity of interconnect, a representative cross-section of wiring fabricated by IBM is shown in the scanning electron micrograph in Fig.2.3. [THE-00] This structure consists of six horizontal layers of interconnect, with vias between each layer. The aluminum material is replaced by copper, fabricated by a dual-damascene process [IBM-97].

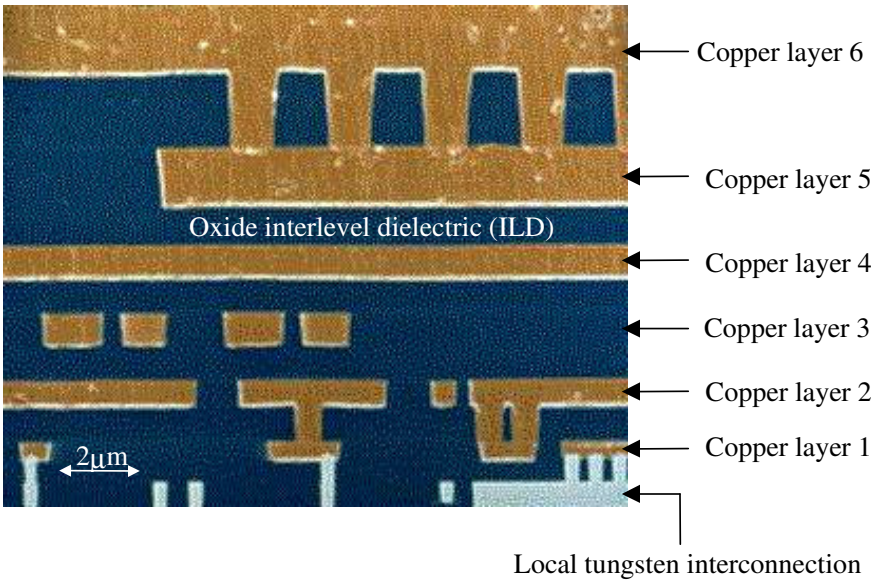


Fig.2.3. Scanning electron micrographs of interconnect architecture with six levels of copper wires/vias, tungsten contacts/local interconnects, and SiO_2 ILD.

Similar to the approach followed for MOSFET transistors, it is worthwhile to explore how interconnect parameters will evolve with scaling of the technology. In order to understand the effects of the interconnect complexity on the chip performance, it is essential to develop a wire-length distribution model. Widely referenced works [DON-81], [CHR-93] modeling wire-length distribution for random logic networks use a well-establish empirical relationship commonly known as Rent's Rule. It may be described by a simple power law:

$$T = kN^{p} \tag{2.1}$$

where T is the number of signal input and output terminals in a logic block, N is the number of gates in a random logic block, k is a proportionality constant, and p (0<p<1) is the Rent's exponent, which denote the degree of wiring complexity. This rule was first described by Landman and Russo in 1971 [LAN-71]. It relates the number of external connections and the number of gates for a given block in a partitioned circuit as is shown in Fig.2.4.

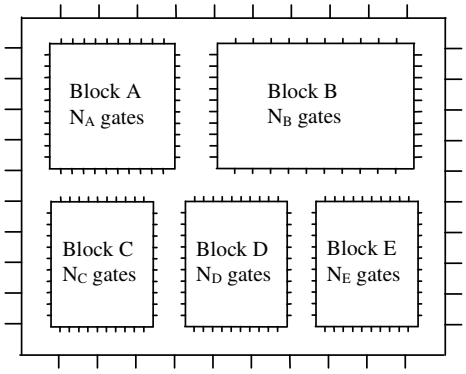


Fig.2.4. Schematic view of logic blocks used for determining wire length distribution.

The correctness of the Rent's Rule has been verified on many real designs. Based on Rent's Rule, Davis et al [DAV-98] presents a new wire-length distribution model, which provides a complete distribution of local, semi global, and global wiring requirements. To determine all the shortest wires in a logic system, they used the recursive property of Rent's Rule. The logic system is divided into logic gates and Rent's Rule is applied to the interconnects between closest neighbor gates. The longer wires are similarly determined by clustering the logic gates in growing numbers until the longest interconnects are found.

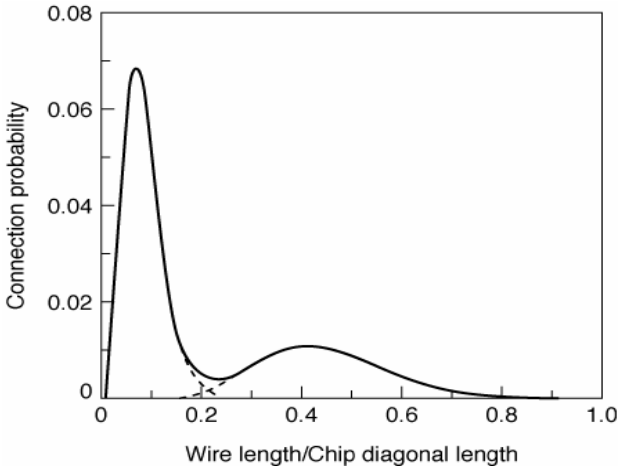


Fig.2.5. A typical distribution of wire lengths in an integrated system.

Kang [KAN-90] observed that the overall wire-length distribution at the system level has a bimodal behavior as shown in Fig.2.5. The distribution has two peaks, the first peak represents local interconnections and the second one represents global interconnections. The local interconnections occupy the first and sometimes the second metal layers in a multilevel system. They usually connect gates, sources and drains in MOS technology. The lengths of these wires tend to scale down with technology. Local interconnects can afford to have higher resistivities than global interconnects since they do not travel very long distances. Semiglobal interconnections are used to connect devices within a block with typical lengths up to 3-4mm. Intermediate wires are wider and taller then local wires to provide lower resistance signal/clock paths.

Global interconnections are generally defined as being all interconnects that occupy the metal levels above the local and intermediate lines. They often travel over large distances, between different devices and different parts of the circuit, and therefore always use low resistance metal tracks. Global interconnects are usually used in power, ground and clock distribution networks. A typical cross-section of a hierarchical “reverse scaling” metallization scheme is shown in Fig.2.6.

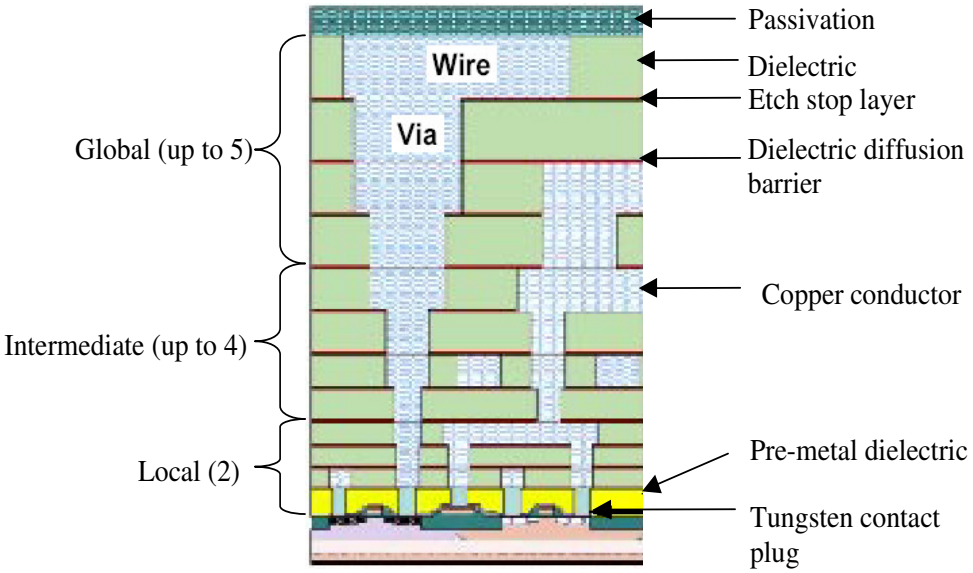


Fig.2.6. Cross-section of hierarchical interconnect structure [ITRS].

To keep pace with density requirements caused by device scaling, interconnect pitch needs to be scaled with every technology generation. Unfortunately, while the gate delay decreases as the feature size is scaled down, the interconnect delay tends to grow due to interconnect resistance, which increases as the interconnect pitch decreases. Jan M. Rabaey [RAB-03] presented different interconnect scaling scenarios shown in Table 2.3.

Table 2.3. *Ideal scaling of wire properties.*

Parameter	Local wire	Constant length	Global wire
Interconnect dimensions	$1/S$	$1/S$	$1/S$
Line length (L)	$1/S$	1	$1/S_C$
Line capacitance (C)	$1/S$	1	$1/S_C$
Line resistance (R)	S	S^2	S^2/S_C
Line response time (RC)	1	S^2	S^2/S_C

Rabaey considered three models: local wires ($S_L = S>1$), constant length wires ($S_L=1$), and global wires ($S_L=S_C<1$), where S_L is the wire-length scaling factor, S is the device scaling down factor and S_C is the scaling factor for the chip size. In first scaling

scenario, which is similar to Saraswat's work [SAR-82], all wire dimensions of the interconnect structure are scaled with the technology factor *S*. This leads to the scaling behavior in Table 2.3. While, the length of local interconnect wires scales with technology by *S,* the length of global interconnect wires is proportional to the die size S_C. It can be seen from Table 2.3. that scaling all cross-section wire dimensions by the factor S, leads to a drastically increased delay time for global interconnects (S^2/S_C), while the delay time for local lines remains constant. In order to illustrate this fact Rabaey shown that the delay of global line goes up with 50% per year for S=1.15 and S_C=0.94, which is in contrast to device internal propagation time, which reduces from year to year. It can be concluded, therefore, that as a result of scaling, interconnects now plays a dominant role in high-performance integrated circuit design.

In order to reduce the dependence of technology scaling on interconnect performance (especially the propagation delay of global lines), Rabaey proposed to scale the wire thickness at a different rate. In the first-order analysis, wire thickness is assumed constant. This "constant resistance" scaling scenario is summarized in Table 2.4, where ε_C (>1) is an extra capacitance scaling factor, that captures the increasingly horizontal nature of the capacitance when wire widths and pitches are shrunk and the height is kept constant [RAB-03]. If ε_C is smaller than the device scaling factor, *S*, the interconnect performance will be improved.

Table 2.4. *"Constant Resistance" scaling of wire properties.*

Parameter	Local wire	Constant length	Global wire
Interconnect dimensions	$1/S$	$1/S$	$1/S$
Interconnect height (T)	1	1	1
Line length (L)	$1/S$	1	$1/S_C$
Line capacitance (C)	ε_C/S	ε_C	ε_C/S_C
Line resistance (R)	1	S	S/S_C
Line response time (RC)	ε_C/S	$\varepsilon_C S$	$\varepsilon_C S/S_C^2$

To illustrate the perspective of on-chip interconnections, the appropriate ITRS predictions are collected in Table 2.5. The ITRS projection for local and intermediate wiring pitch is close to 4-5λ, and 5-6λ respectively, and is around 8-9λ for minimum

wiring pitch at global metal layer. λ is one half of the "minimum" mask dimension, typically the length of a transistor channel. The number of metal layers will increase from 8 at the 0.107μm node to 11 at the 0.025μm technology node for enhanced connectivity. While the ITRS predicts a reduction of the effective dielectric constant from 3.0-3.6 to about 1.8 in 2016, the copper remains as the conductor material with the smallest available 2.2μΩ-cm effective resistivity. This leads to a slow decrease in the wiring capacitance (low dielectric constants) and an increase in the wiring resistance, despite increases in the aspect ratio A/R (ratio of metal thickness to metal width).

Table 2.5. *The most important interconnect parameters according to ITRS roadmap.*

Year of production	2003	2005	2007	2010	2013	2016
Minimum feature size [nm]	107	80	65	50	35	25
Number of metal levels	8	10	10	10	11	11
Total interconnect length [m/cm^2]	5788	9068	11169	15063	22695	33508
Local wiring pitch [nm]	245	185	150	105	75	50
Local wiring A/R (for Cu)	1.6	1.7	1.7	1.8	1.9	2
RC delay (1mm line) [ps]	176	256	342	565	970	2008
Intermediate wiring pitch [nm]	320	240	195	135	95	65
Intermediate wiring A/R (for Cu)	1.7	1.7	1.8	1.8	1.9	2.0
RC delay (1mm line) [ps]	101	155	198	348	614	1203
Global wiring minimum pitch [nm]	475	360	290	205	140	100
Global wiring A/R (for Cu)	2.1	2.2	2.2	2.3	2.4	2.5
RC delay (1mm line) [ps]	40	59	79	131	248	452
Conductor resistivity [μΩ-cm]	2.2	2.2	2.2	2.2	2.2	2.2
Dielectric constant	3.0-3.6	2.6-3.1	2.3-2.7	2.1	1.9	1.8

2.4 THE INTERCONNECTION CRISIS.

2.4.1 Power consumption

With the high density of integration and high clock rates, advanced microprocessors dissipate a significant amount of power in a very small physical area. On-chip power dissipation is important in two respects: absolute power consumption, and power density.

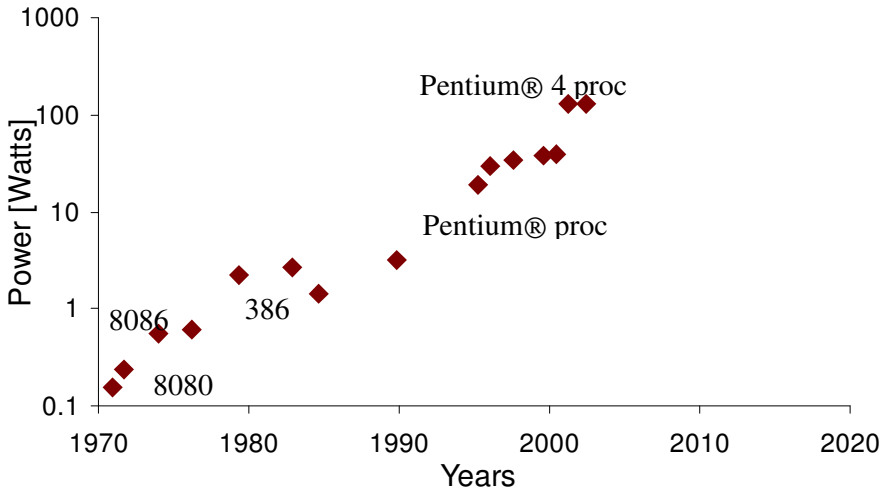


Fig.2.7. Power trends in Intel family processors.

Fig.2.7. shows the absolute power consumption of representative Intel microprocessors as a function of time. It is clear from this figure that the overall trend is the exponential increase in power dissipation with time. This trend is not particular to one company's technology but is true for all microprocessor corporations. There are two main reasons why the power consumption increases: speed and the number of gates on the silicon wafer. Since a single chip processor in production consume more then 100W of power, thermal management is a major concern. The power density affects local and overall chip temperature, which adversely affects long-term reliability and life time of electronic devices. With increasing device densities and operating frequencies, the density of power that is generated on-chip increases. Chips today operate at 85-120°C due to

device and interconnect heating. The relationship between the reliability and the operating temperature of a typical silicon semi-conductor devices shows that a rise in the temperature corresponds to an exponential decrease in the reliability and life expectancy of the devices. This issue imposes increasing demands on already expensive packaging solutions to transport heat away from the chip in order to prevent quiescent temperatures.

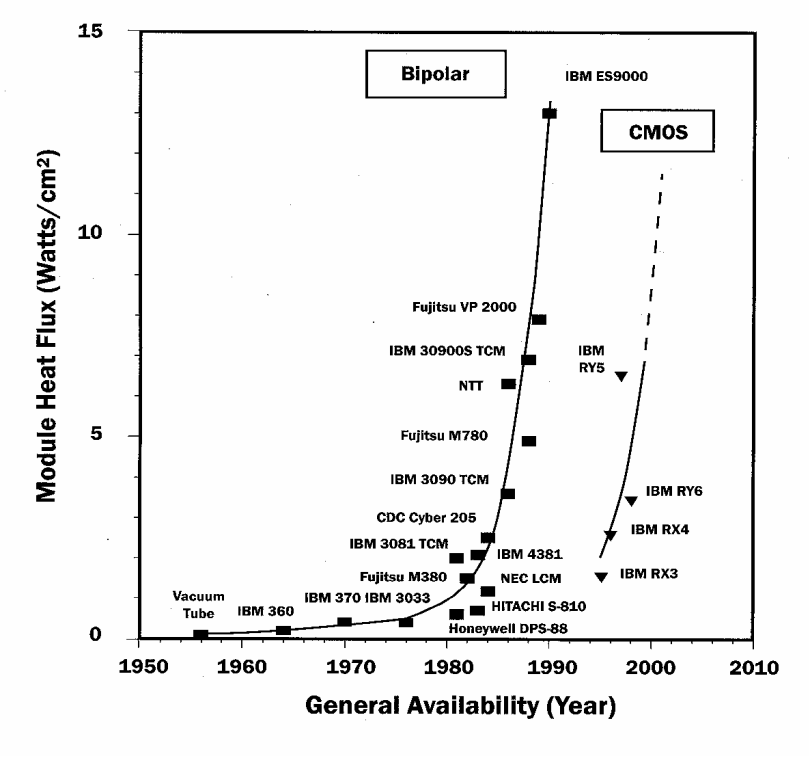


Fig.2.8. Heat flux for the Bipolar and CMOS technologies [CHU-99].

In many areas of electronics applications, the barriers resulting from this limitation have been already encountered influencing essentially their further developments. The history of computer evolution shown in Fig.2.8 is a very spectacular example of that [CHU-99]. The increase of the computer power is inherently connected with the larger heat dissipation due to self heating. The increase of the heat dissipation density for bipolar technology reached a dramatically high level at the end of eighties, becoming the real barrier to further progress. The introduction of CMOS technology was a true breakthrough for the computer development, but it gave a 10-year shift of the problem as is indicated by the CMOS curve in the Fig.2.8.

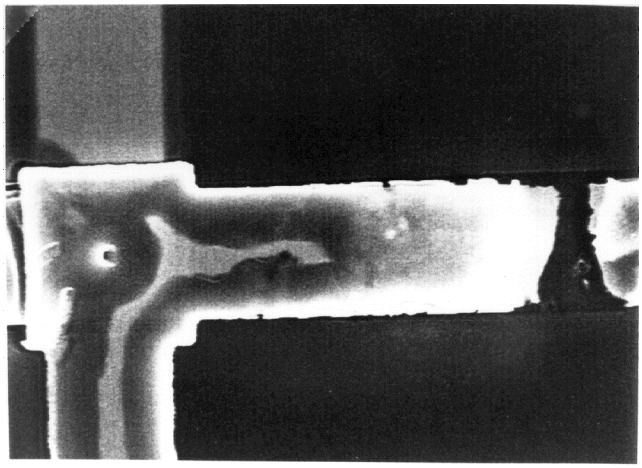


Fig.2.9. A wire broken off due to electromigration [RAB-03].

Another serious problem reported by the literature [BAN-99], [BAN-00], [IM-00], [BAN-01] is the interconnect reliability due to the thermal effects, which is an inseparable aspect of signal transmission through interconnect. The self-heating of interconnect, which is caused by the flow of current is becoming a serious desisgn issue, particularly for global interconnects. Interconnect self heating and low thermal conductivity of dielectric materials will strongly impact the magnitude of the maximum temperature within future integrated circuits. This leads to the electromigration effect shown in Fig.2.9, which is dependent on temperature and finally may decrease the interconnect reliability and interconnect lifetime. It can be concluded that, due to natural limits in thermal management, the power consumption in modern integrated circuits will become a real barrier to its further progress.

2.4.2 Propagation time.

Signal timing becomes a greater problem as silicon circuits improve and clock rates increase. The popular graph shows Fig.2.10. and taken from the 2001 ITRS, illustrates the relative delay time for gate, local and global lines versus feature size. It shown the growing gap between the wire and gate performance.

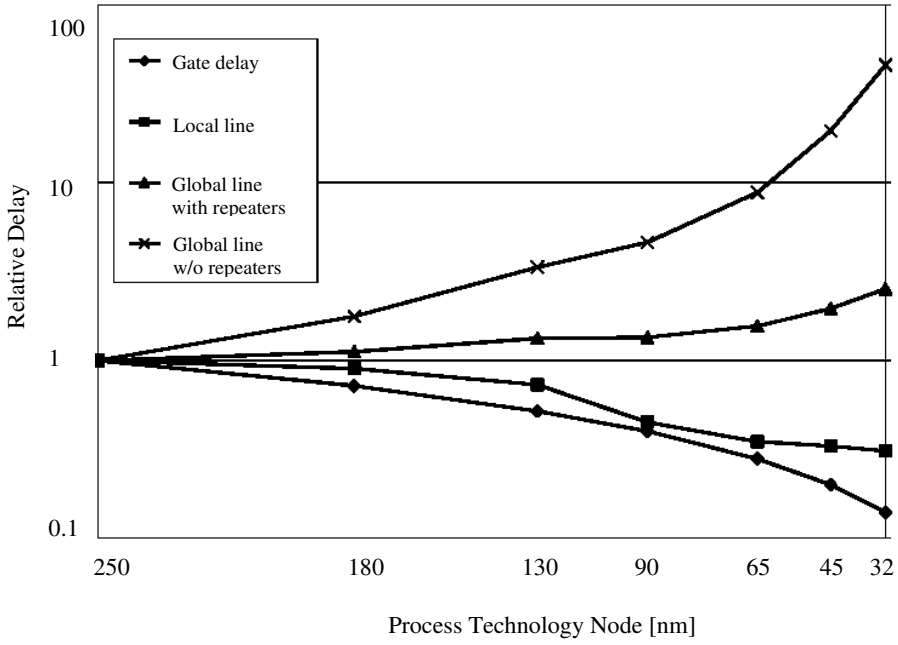


Fig.2.10. Gate and wire scaling, from 2001 roadmap.

Implementation of copper and low-k materials allows scaling of the local and intermediate wiring levels and minimizes the impact of wiring delay. Because of the shrunk line length the local wiring levels are relatively unaffected by traditional scaling. In the case of global lines, the benefit of materials changes is insufficient to meet overall performance requirements and the global RC delay tends to grow. The latency of global interconnect becomes too high to send data across a microprocessor within a single clock cycle, which can limit the maximum operating frequency of modern IC's. It can be concluded that the interconnect delay is becoming higher than the gate delay and becomes the dominant factor determining the overall device speed.

2.4.3 Capacity limitations.

The bandwidth for data transmission on global interconnect lines, is decreasing as integrated circuits technology is scaled. Bandwidth is decreasing due to a migration to smaller dimensions and a corresponding increase in clock frequency. Miller and Ozaktas

[MIL-97] have shown that the maximum number of bits per second that can be carried by a simple electrical interconnection is:

$$B \approx B_o \frac{A_{Int}}{L_{Int}^2} \tag{2.2}$$

where A_{Int} is the cross-section area of the conductor, L_{Int} is the interconnection length and B_o is $\approx 10^{16}$ for copper or aluminum on-chip interconnect at room temperature. Note that this limit is scale-invariant. It only depends on the ratio of the cross-sectional area of the wiring to the square of its length A_{Int}/L_{Int}^2. Taking the simplest approach to CMOS scaling and reducing all the dimensions of a system, the circuit performance increases but the interconnect aspect ratio, and therefore its capacity, is left unchanged. Thus, electrical interconnects cannot keep up with the device performance enhancements provided by scaling, and the problem is worse for high-aspect ratio global and off-chip wires. Such a limit will become a problem as microprocessors approach Tb/s information bandwidths. The limit will particularly affect architectures in which one processor must communicate reasonably directly with many others.

2.5 NEW POTENTIAL SOLUTION.

2.5.1 Conductor potential solution.

In the past, most semiconductor manufacturers have used aluminum interconnects for their devices. Although aluminum is a good conductor, it becomes less practical to use, because of size limitations, as semiconductor processes shrink to 0.15 and 0.13µm. To overcome this limitation, alternative metallization based on metals with lower resistivities are needed. Table 2.6 lists several new candidates for conductor materials. Among the presented metals, it can be seen that only copper (Cu), silver (Ag), and gold (Au) have resistivities lower than aluminum. In the last few years, extensive research has been carried out on Cu based metallizations [NGU-99], [KAP-02] and [BAN-00]. Typically, using

copper instead of aluminum reduces interconnect resistance by 40%, resulting in better signal integrity, smaller propagation delays, lower power dissipation, and higher performance. Additionally, the electro-migration properties of copper are also better than those of aluminum. The latter means that higher current densities can be allowed in copper leading to higher integration densities.

Table 2.6. *Low bulk resistivity materials.*

Material	ρ(Ω-m)
Silver (Ag)	$1.6*10^{-8}$
Copper (Cu)	$1.7*10^{-8}$
Gold (Au)	$2.2*10^{-8}$
Aluminium (Al)	$2.7*10^{-8}$
Tungsten (W)	$5.5*10^{-8}$

Although the benefit of using copper as interconnect material is obvious, there are difficulties in the patterning of copper. Wet etching is not useful for patterning sub-micron structures due to its isotropic nature. Reactive ion etching (RIE) of copper is also not practical because of the lack of volatile copper compounds at low temperature [HOW-91]. Damascene technology using chemical mechanical polishing (CMP) is the only technology known to be able to pattern copper with a large process window [KAA-91].

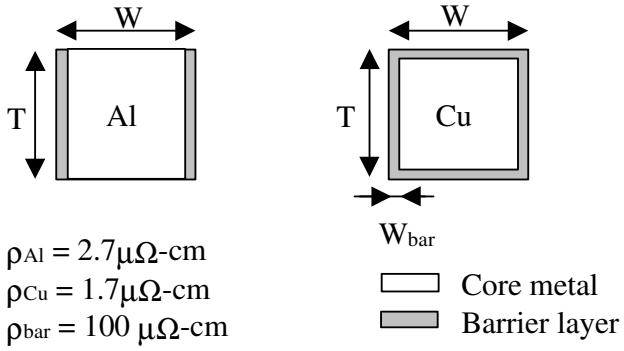


Fig.2.11. Basic differences between the formation of aluminum and copper interconnections.

Fig.2.11. illustrates the RIE metal-patterned Al and damascene-patterned Cu based interconnect. The effective sheet resistance of copper wiring depends on the barrier material and may reach values close to 2.2μΩ-cm. As metal lines are scaled to below 100nm, resistivity begins to increase substantially. This increase is primarily controlled by a scattering mechanism due to the properties of surface and interfaces of copper film [BUC-02]. This effect is severe enough to negate the inherent benefits of copper metallization. One potential solution that will give some modest lowering of copper resistivity, is elimination of Cu barriers through the modification of low dielectric constant materials to prevent Cu diffusion. More significant reduction of Cu resistivity may be achieved through lowering the chip temperature.

2.5.2 Dielectric potential solution.

As device dimensions shrink, propagation delay, crosstalk noise and power dissipation due to resistance-capacitance (RC) coupling become significant due to increased wiring capacitance, especially interline capacitance between the metal lines on the same level. These factors all depend critically on the dielectric constant of the separating insulator. Since the interconnect capacitance is proportional to the dielectric constant of the insulator material it can be effectively reduced by using materials with a lower dielectric constant [IDA-94].

Table 2.7. *Example of low-k dielectric materials.*

Material	Film Types	k-Range
Fluorinated Silicate Glass (FSG)	Oxide	3.2-3.6
Polyimides	Organic	3-3.5
Hydrogen Silsesquioxane (HSQ)	Oxide	2.8-3
Methyl Silsesquioxane (MSQ)	Oxide	~2.7
PTFE (Teflon)	Fluorinated	~1.9
Porous Inorganics	Porous	1.8-2.2
Porous Organics	Porous	<2.2

Changing from aluminum to copper reduces the metal resistance by approximately 40%, and changing from a standard SiO_2 dielectric material to a low-k dielectric can reduce the capacitance by as much as 50% [GAR-02]. The improvement of dielectric constant depends of course upon the materials selected. Table 2.7 lists several example of low-k dielectric materials. There are organic and inorganic materials spanning a wide range of dielectric constant. Among these dielectrics, only a limited number have been introduced into production due to integration and reliability issues [HAV-01]. Integration of low-k materials is directly related to optimizing different tradeoffs between material properties, device architectures, and process flows. The three major aspects that determine the future of low-k material integration are dielectric constant, process cost and process reliability. The ultimate solution for any particular node will be determined by the best compromise between these 3 factors. The ITRS predict that Cu and low dielectric constant materials continue to find applications in future generation technology, but for long global wiring, radically new interconnect solutions will be required.

2.5.3 Alternative interconnect approaches.

It becomes evident that the electrical interconnections of on-chip and chip-to-chip systems are approaching or have reached their fundamental limits and represent the present performance bottleneck. In order to realize gigascale integration (GSI) a variety of technological and architectural barriers must be overcome. The new materials proposed by the ITRS to increase the speed of interconnects are insufficient. However, because these solutions only partially solve the interconnect problem and have penalties, they are likely to only extend the life of the existing paradigm by a few years. It can be concluded, that to meet the performance challenge, revolutionary approaches will be needed.

One possible physical approach to improve electrical interconnections, is to cool the chips and/or circuits (to get lower resistance in lines), e.g., to 77 K, or using superconducting lines. Since, cryogenic cooling dramatically reduces the resistivity of both aluminum and copper interconnect, wiring materials with vanishingly small resistivity are possible. Cooling to low room temperatures is already implemented in some computers. Cryogenic cooling would be physically possible with current technology. Superconducting

materials are still not available for room temperature, and the use of superconductors would also require significant cooling; unless temperatures <77K are used. Consequently, practical, room-temperature superconductor materials would have to be developed.

Another approach are a RF (*Radio Frequency*) or wireless interconnect technologies, which have been recently considered as viable candidates for on-chip, or more likely for off-chip interconnects [CHA-01], [SHI-02]. The RF technology is divided into the categories of free-space transmission and guided-wave transmission. The bandwidth of RF approaches, is only limited by the bandwidths of the transmitting and receiving components, and not by the transmission medium. However, the efficient transmission and receiving of RF/microwave signals in free space require the size of antennas to be comparable with their wavelengths. Even for the operating frequency as high as 100 GHz the optimal aperture size of the antenna is on the order of 1 mm, which is too large to be comfortably implemented in the future VLSI. RF interconnects have some difficult challenges to overcome before becoming a viable candidate to replace global wires. First of all, power dissipation of RF solution must be reduced and the silicon area consumed by RF circuits must be less (area required by coupling capacitor is ~600μm^2).

There is also a low-swing interconnect approach [ZHA-98], [ZHA-00], which assumed that by reducing the voltage swing of interconnect lines, it is possible to drastically reduce the energy consumption. However, these schemes tend to be slow and decreases the noise margin, which is a concern in low supply voltages (below 1.8V).

Much easier approach, is to use optical interconnections, which may constitute a suitable alternative to overcome these constraints. Optoelectronic interconnections has known advantages such as large information capacity, no electromagnetic wave interference, high interconnection density, low power consumption, high speed, and planar signal crossing. Optical interconnections are thus a very attractive solution to solve on-chip global electrical interconnect problems. However, before optical interconnects become a reality, the cost versus performance trade-off must clearly favor such a paradigm shift.

2.6 CONCLUSION.

Silicon integrated circuit technology has evolved rapidly, driven by continual increase in device functional density. Understanding future device and interconnect limits

is necessary to determine the best opportunities for future microprocessors. This chapter, based on the ITRS roadmap, has reviewed the current and future trends in device and interconnect technology. While traditional transistor scaling allows to meet future system requirements, interconnect scaling has become the performance-limiting factor for new designs. The impact of technology scaling on the power consumption, propagation time and interconnect capacity have been presented. It was shown that many practical and fundamental limits are being approached, and the substantial changes to interconnect technologies will be required. Current solutions, such as the low-resistivity copper and low-permittivity dielectrics have been also described. However it can be concluded that to meet the performance challenge, revolutionary approaches will be needed.

III. Electrical Clock Distribution Network

Chapter III

Electrical Clock Distribution Network

3.1 INTRODUCTION

Semiconductor technologies operate at increasingly higher speeds, and system performance has become limited not by the delays of the individual logic elements but by the ability to synchronize the flow of the data signals. A clock network distributes the clock signal from the clock generator, to the clock inputs of the synchronizing components. This must be done while maintaining the integrity of the signal and minimizing (or at least upper bounding) the following clock parameters: the clock skew, the clock slew rate, the clock phase delay and the sensitivity to parametric variations of the clock skew. Additionally these objectives must be attained while minimizing the use of system resources such as power and area. The clock distribution network of a modern microprocessor uses a significant fraction of the total chip power and has substantial impact on the overall performance of the system. Typical power dissipation in the clock distribution network is one third of the total power dissipated in CMOS VLSI systems [GRO-98], [KAW-98], [BAI-98], [TAM-00] and can even constitute more then half of the total power dissipated in some designs.

3.2 CLOCK SYSTEM PARAMETERS.

The primary purpose of a clock distribution network is to regulate the flow of information between different portions of the chip. This section provides an overview of the terminology and issues involved in the design and simulation of a clock distribution network in modern integrated circuits

3.2.1 Clock skew.

Generally, a synchronous digital system consists of a series of registers between which are blocks of combinational logic. A schematic diagram of a generalized synchronized data path is presented in Fig.3.1. [FRI-95], where C_i and C_j are the clock signals driving the sequentially-adjacent pair of registers R_i and R_j respectively.

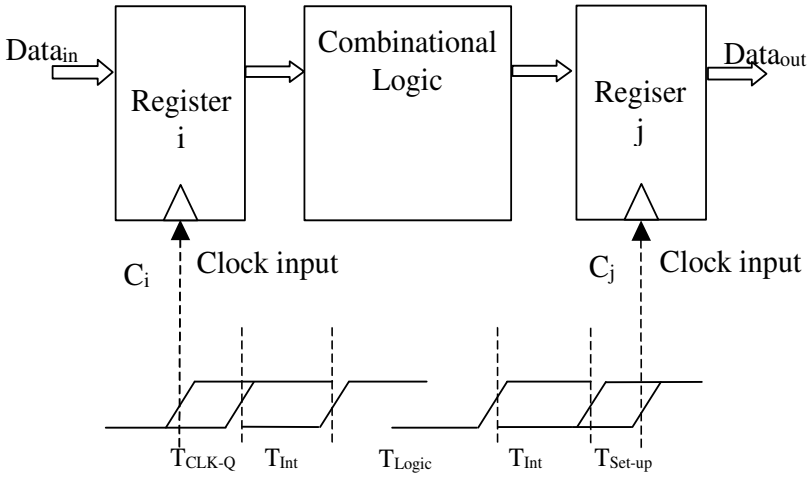


Fig.3.1. Delay components of a clocked data path

The maximum possible clock frequency f_{CLKmax} between any two registers in a sequential data path through which a synchronous digital system can move data is given by.

$$\frac{1}{f_{CLKmax}} = T_{CP(min)} \geq T_{Skew} + T_{PD} \qquad (3.1)$$

where $T_{CP(min)}$ is the minimum allowable clock period, T_{Skew} is the clock skew, and T_{PD} is the total path delay between two sequentially-adjacent registers described as:

$$T_{PD} = T_{CLK-Q} + T_{Logic} + T_{Int.} + T_{Set-up} \qquad (3.2)$$

The total path delay T_{PD} is the sum of the time required for the data to leave the register when the positive edge of the clock arrives ,T_{CLK-Q}, the time necessary to propagate through the logic T_{Logic}, and interconnect T_{Int}, and the necessary setup time that must be met at the final register to guarantee correct operation, T_{Set-up}. If either of these time conditions is not met, the functionality of the system will be compromised.

The clock skew T_{Skew}, directly associated with maximum clock frequency (Equation (3.1) is defined as the maximum difference in clock signal arrival times between two sequentially-adjacent or shared direct communication any registers, as shown in Fig.3.2.

$$T_{Skew} = T_{Ci} - T_{Cj} \tag{3.3}$$

If the clock signals C_i and C_j are in complete synchronism (i.e. the clock signals arrive at their respective registers at exactly the same time) the clock skew is zero. The presence of clock skew can severely limit the performance of a synchronous system.

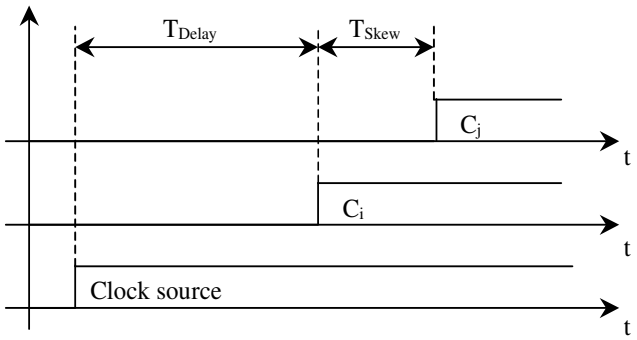


Fig.3.2. Timing diagram of clocked data path.

It should be noted that the clock skew can be a negative or positive value, as is shown in Fig.3.3. If the clock signal arrives at the first register before it reaches the second register then $T_{Ci} - T_{Cj} > 0$ and there is said to be positive clock skew. In the opposite case when $T_{Ci} - T_{Cj} < 0$, the clock skew is defined as being negative.

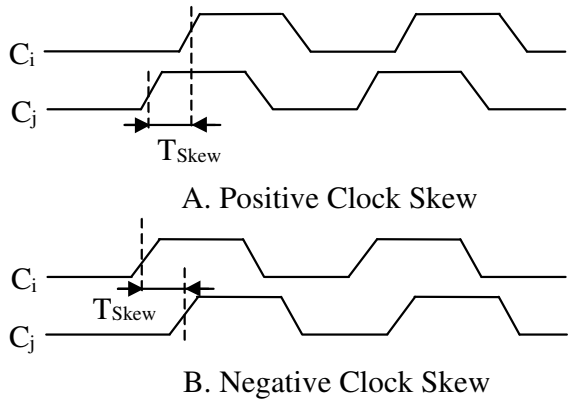


Fig.3.3. Clock timing diagram.

Positive clock skew serves to increase the path delay which leads to a decrease in the maximum available clock frequency. As a result, system performance is degraded. Negative skew, on the other hand, can improve the performance of synchronous system by decreasing the delay of a critical path. However, the existence of negative clock skew in a path imposes a constraint on the minimum path delay. It should be noted that the positive and negative conventions are applicable only relative to the direction of data flow.

Sources of clock skew

The challenge to designers of clock distribution networks is how to control system clock skew, so that it becomes an acceptably small fraction of the system clock period. As a rule, most systems cannot tolerate a clock skew of more than 10% of the system clock period. If the system clock skew goes beyond the design limit, system behavior can be affected. In order to minimize the clock skew, it is first necessary to understand its sources. There are a variety of possible factors that can cause clock skew. Wann and Franklin [WAN-83] reported the following sources of skew in clock distribution networks:

- Differences in line lengths from the clock source to the clocked register.
- Differences in delays of any active buffers within the clock network.
- Differences in passive interconnect parameters, such as line resistivity, dielectric constant and thickness, via/contact resistance, line and fringing capacitance, and line dimensions.

- Differences in active device parameters, such as MOS threshold voltages and channel mobilities, which affect the delay of the active buffers.

The amount of clock skew depends on the design itself as well as process variations. There are several methods to reduce the impact of the process and system variations on the clock network timing relationship. The most common clock distribution method is to insert buffers at the clock source and/or along a clock path, forming a symmetrical H-tree structure, this will be described in more detail in the next sections.

3.2.2 Clock power dissipation

The next very important issue in the design and optimization of a clock distribution network is the clock power dissipation. The clock distribution network of a modern microprocessor uses a significant fraction of the total chip power and has substantial impact on the overall system performance. In a modern VLSI circuit with power consumption of 100W [KUR-01], [GRO-02] the clock tree uses at least one third or more of this power [BOB-92].

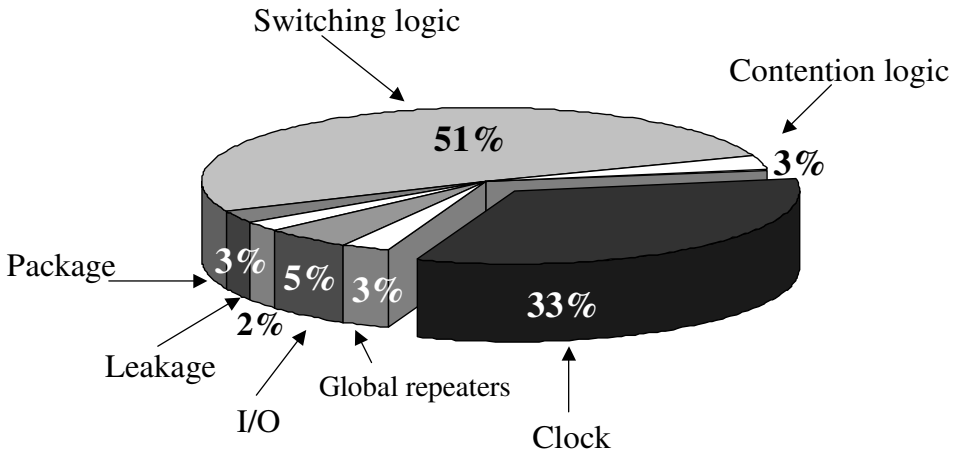


Fig.3.4. Approximate power breakdown of the Intel Itanium microprocessor.

Fig.3.4. shows the approximate power breakdown of the Intel Itanium microprocessor [NAF-02]. Since the clock network consume 33% of total power dissipated

in the system, thermal management becomes a major concern. One of the reason for such large power consumption of the clock system is that the transition probability of the clock system is 100%, while that of the ordinary logic is about one-third on average [KAW-98].

The power consumption in VLSI CMOS chips have been the subject of many work [KAN-86], [LIU-94], [VEM-94], [GUP-00]. As is shown in Fig.3.5. the power dissipated by a clock distribution network can be divided into three sources.

$$P_{Total} = P_{dynamic} + P_{short\text{-}circuit} + P_{leakage} \tag{3.4}$$

The first and the most significant contributor to energy consumption is the average dynamic power dissipation attributed to the charging and discharging the parasitic capacitances associated with the clock interconnects, active buffers and a gates of timing elements as is shown in Fig.3.5.

$$P_{dynamic} = \alpha f C_{Total} V_{dd}^2 \tag{3.5}$$

Where α is the activity factor (for clock system α=1), f is the operating frequency, C_{Total} is the total clocked parasitic capacitance and V_{dd} is voltage supply.

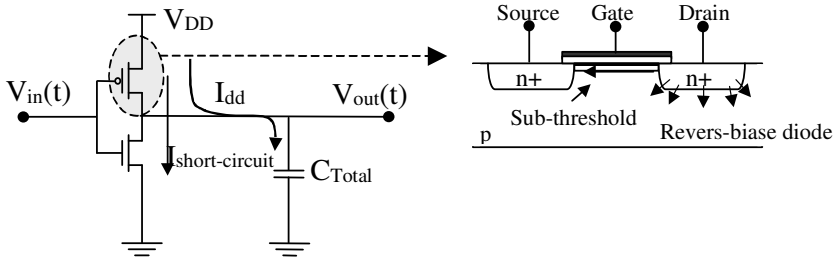


Fig.3.5. Power dissipation mechanisms in CMOS technologies.

Short-circuit power dissipation, $P_{short\text{-}circuit}$, is caused by the fact that in the CMOS gates there is a period when both the NMOS and PMOS devices are simultaneously conducting. When it occurs, there is a direct open path for current from supply to ground,

and a short-circuits current exists. The energy dissipated due to short-circuit current I_{sc} is dependent on input and output slopes of the signal, supply voltages, and device parameters.

$$P_{short\text{-}circuit} = I_{sc} V_{dd} \tag{3.6}$$

Leakage power, $P_{leakage}$, is dissipated even when there is no circuit activity. There are two sources of leakage power in CMOS circuits. The first source, reverse-bias diode leakage, occurs when the drain-to-bulk voltage of either the PMOS or NMOS transistor is reverse biased. The second source, sub-threshold leakage occurs when the gate-to-source voltage of the device is below threshold voltage, but is large enough to put the device into weak inversion. Consequently the transistors do not turn off completely.

$$P_{leakage} = I_{leakage} V_{dd} \tag{3.7}$$

For CMOS VLSI the primary component of power dissipation is dynamic power. It is possible to reduce fV^2C dynamic power by lowering the clock frequency, the power supply, and/or the capacitance load of the clock distribution network. Lowering the clock frequency, however, conflicts with the primary goal of developing high speed VLSI systems. Therefore, for a given circuit implementation, low dynamic power dissipation is best achieved by employing certain design techniques that minimize the power supply and/or the capacitance load [MAN-94], [NEV-95], [VIT-97], [ATH-00].

3.3 CLOCK DISTRIBUTION DESIGN

Techniques for synchronous VLSI often utilize a tree and grid-like structure with several levels of hierarchy as shown in Fig.3.6. It represents the most efficient solution in terms of skew covering the symmetric topology on the upper metal levels. The clock topology is partitioned into three segments. The first component is the phase-locked loop (PLL). By anticipating the edges of the input, the PLL can generate new clocks with edges slightly earlier than the input clock. By tuning the amount of time, these new clock edges

precede the input clock edge to the delays of the various clock tree branches. As a result, all registers will see the clock edge at about the same time.

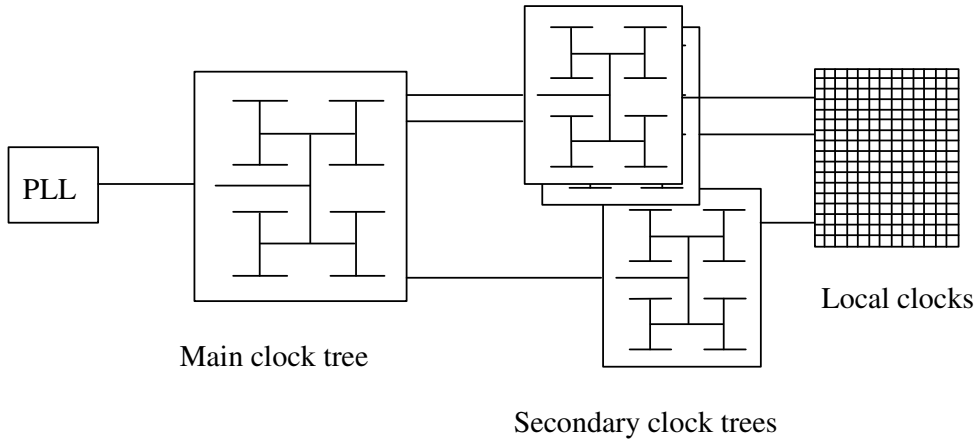


Fig.3.6. An example of a clock distribution network.

The basic concept of a PLL reduces the overall clock network delay and minimizes clock skew. The second component of a CDN is the global clock network, which distributes the clock signal across the chip. The global CDN is usually placed on the upper metal layer and utilizes a tree-like structure. The optional secondary clock trees connect global and local clocks and are placed on intermediate metal layers. The last component of the CDN are the local clocks. These clocks provides the clock signal to the clocking registers. They are usually placed on the first metal layers and utilize grid-like structures.

3.3.1 Clock distribution trees.

Since controlling the clock signal is critical to the operation of high performance systems, a great deal of engineering goes into its proper generation and distribution. The most common strategy for distributing the clock signal is to use a tree-like structure with several levels of hierarchy illustrated in Fig.3.7.[FRI-95]. This is required to cope with the inherently large fanout associated with the clock signal. The clock input is connected to the ”*trunk*” and the signal is subsequently split and distributed to each major ”*branch*”. Each major branch feeds the signal to two or more smaller branches. This process continues

until enough minor branches are formed so that the signals can be used to directly clock storage or logic elements (”*the leaves*”). The metaphor for describing a clock distribution network as a tree (e.g. ”*trunk*”, ”*branch*”, ”*leaves*”) is commonly accepted and used throughout the literature. The most prevalent approach remain the basic ”tree” structure or variations of it.

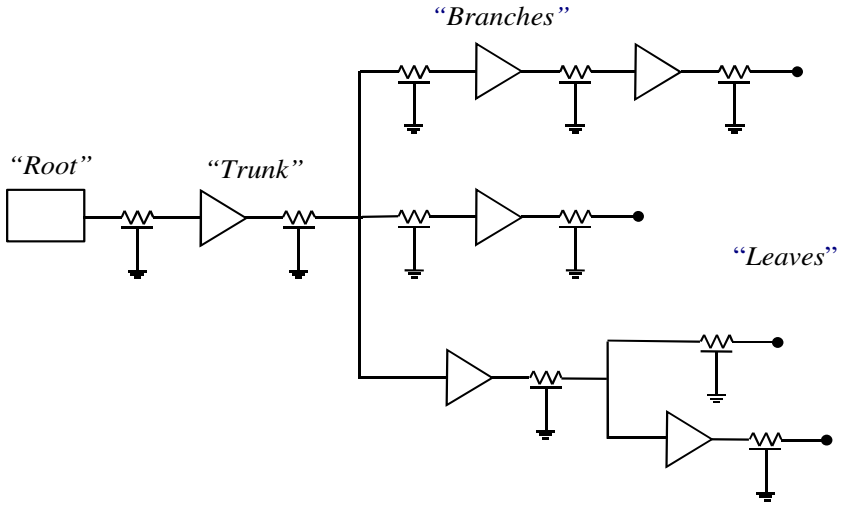


Fig.3.7. Tree-like structure of clock network.

In a high-performance VLSI, especially in a global clock network, each wire is shielded at the sides by power and ground lines (Fig.3.8). This results in predictable capacitive and inductive characteristics, which allow control of the delay of each clock signal path and minimization of the skew between these paths. The shielding also reduces noise coupled into nearby signal lines from the clock lines [AVE-99].

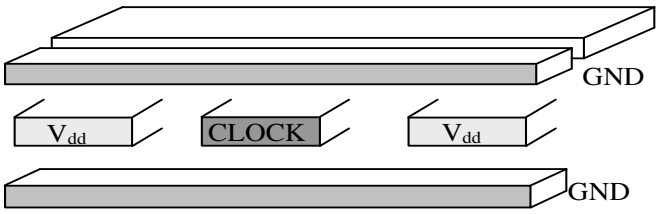


Fig.3.8. Clock wire shielding.

3.3.2 Buffered clock tree.

By far the most popular method for distributing clock signals in VLSI applications is to insert buffers at the clock source and/or along a clock path, forming a tree structure. There are three principal reasons for the use of distributed buffers [WAN-83].

- In complex circuits, various clock subcycles and pulses derived from the main two clock phases may be needed. In this situation logic and buffers are needed to obtain these signals and distribute them within the chip.
- Distributed buffers are used to amplify the clock signals degraded by the distributed interconnect impedances.
- The local clock nets need to be insulated from upstream load impedances.

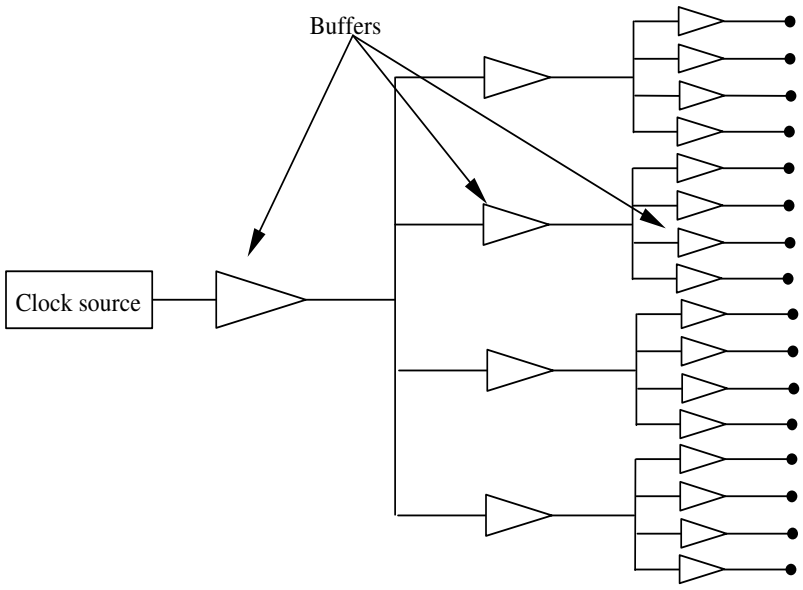


Fig.3.9. Buffer-tree clock distribution representation.

Fig.3.9. presents the organization of a buffered clock tree network. This approach becomes necessary when the layout is large because it would be impossible to get the clock signal distributed fast enough through the long clock lines without feasible sized clock-buffers. In such clock trees there are two ways of inserting the buffers. One is to use minimum sized buffers placed at equi-distant positions (often they are placed individually in each branch in the tree). The other way is to use cascaded buffers with different driving

capability. The number of buffer stages between the clock source and each clocked register depends on the total load capacitances (in the form of registers and interconnect) and permissible clock skew. It is also essential that every buffer stage drives the same number of fan-out gates so that the clock delays are always balanced. The final buffer along each clock path provides the clock signal to the clocked registers.

On the other hand there are some facts that motivate the minimizing of the number of buffers used in the clock distribution network:

- Buffers in clock trees introduce two additional sources of skew: the first source is the effect of process variations on buffer delays, the second source is the imbalance in buffer loading.
- In high-speed designs the number of buffers may be large enough to determine the total chip area.
- The total capacitance and therefore the total power consumed in clock system depends on the number of buffers.

3.3.3 Clock tree networks.

3.3.3.1 Grid.

The clock grid is the simplest clock-distribution structure which is commonly used in the Alpha series of microprocessors, produced by Digital Equipment Corp (Hudson, MA). The grid based technology is essentially a grid of wires that are driven by one or more buffers as shown in Fig.3.10. The grid provides a constant regular structure so the clock signal may be easily distributed near to every location where it may be needed. The granularity of the grid is directly connected to the distribution of the clock loads. The grid reduces local skew by connecting nearby points directly. Additionally, the clock grid ensures a universal availability of the clock signal, good process-variation tolerance and an easy design process. Disadvantages with this approach are that the grid wires increase the total capacitive load of the clock network, which in turn increases the power consumption.

Additionally the clock grid is an area-inefficient solution. The clock grid is typically used in the final stage of the clock distribution network

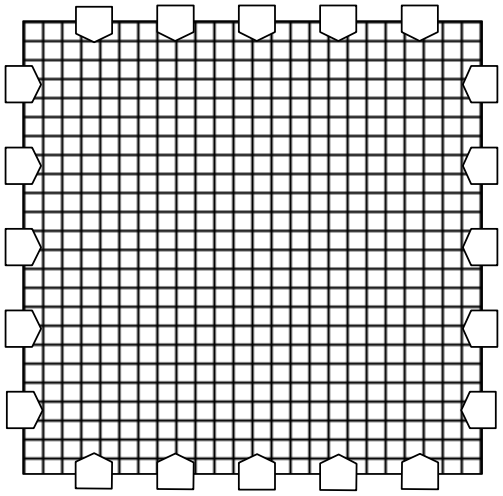


Fig.3.10. Grid based topology.

3.3.3.2 Symmetrical H-tree.

Since clock skew is due to unequal clock path lengths, it is very desirable to eliminate this skew by using fully symmetrical structures like H-tree and X-tree. Fig.3.11. shows the hierarchy of a commonly used planar H-tree. It is obvious from this figure that the paths from the clock signal source to the clocked register of each clock path are identical and therefore clock skew is minimized.

In the H-tree network, the primary clock driver is connected to the center of the main ”H” structure. The clock signal is transmitted to the four corners of the main H-shaped structure. These four close-to-identical clock signals provide the inputs to the next level of the H-tree hierarchy, represented by the four smaller ”H” structures. Using this basic concept, the H-tree distribution scheme repeats an H-shaped structure recursively until a small enough subblock is obtained. The final destination points of the H-tree are used to drive the local registers. For regular networks, the H-tree is a structured approach to clock distribution design. It has the property that the clock entry point for every subblock is the same distance from the clock source and, in theory, has practically the

same delay, which gives a skew-free implementation. As a result, the amount of clock skew that is introduced within each subblock of the design is proportional to the block size. The maximum block size can be determined from the maximum allowable skew. Typically the H-tree is driven by a huge staged buffer. Note that strict adherence to the H-tree structure requires a highly structured design and hence is directly applicable only to highly structured, repetitive circuits. Of course, attempts can be made to approximate it in less structured circuits.

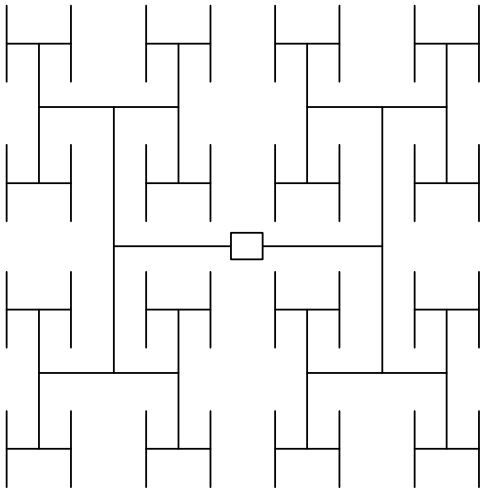


Fig.3.11. H-tree topology.

The primary delay difference in a clock signal paths in symmetrical H-tree is due to variations in process parameters that affect the interconnect impedance and in particular any active distributed buffer amplifiers. Choosing the H-tree it must be taken into account that the interconnect capacitance (and therefore the power dissipation) is much greater for the H-tree as compared with the standard clock tree, since the total wire length tends to be much greater [SOM-93]. This increased capacitance of the H-tree structure exemplifies an important tradeoff between the clock delay and the clock skew in the design of the high speed clock distribution networks. Symmetric structures are used to minimize clock skew, however, an increase in clock signal delay is incurred. Additionally, symmetrical structures are difficult to implement in practice due to routing constraints and different fanout requirements.

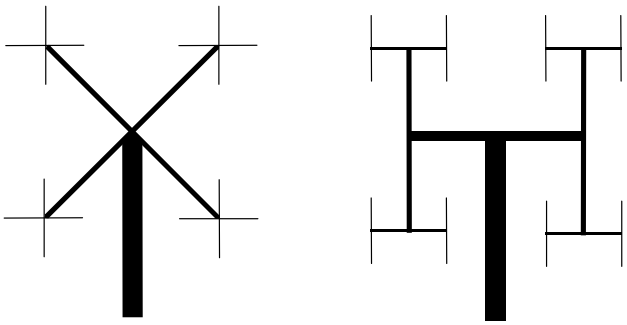


Fig.3.12.Tapered X-tree and H-tree clock structures.

In high-speed clock distribution networks, the reflections from the branching points in the clock tree must be considered. If the lines are not designed properly, reflections may disturb the clock signal. To avoid such situations, the impedance of the conductor leaving each branch point Z_{k+1} must be twice the impedance of the conductor providing the signal to the branch point Z_k for an H-tree structure, as shown in Fig.3.12. [BAK], [KEE-92]:

$$Z_k = \frac{Z_{k+1}}{2} \tag{3.8}$$

and four times the impedance for an X-tree structure

$$Z_k = \frac{Z_{k+1}}{4} \tag{3.9}$$

As a result, in parallel, they will act as a single line with the same impedance as a incoming line. This matching condition can be accomplished by narrowing down the line width at the branching points because the characteristic impedance of a line, Z, is inversely proportional to its capacitance.

$$Z = \sqrt{\frac{L}{C}} = \frac{1}{\upsilon C} \tag{3.10}$$

where: υ-is the propagation speed of the electromagnetic waves in transmission line medium, L and C are interconnect inductance and capacitance respectively.

3.4 EXAMPLE IMPLEMENTATION OF CLOCK DISTRIBUTION NETWORKS.

Many approaches to high-performance fully synchronous intra chip clock distribution networks for high-performance gigascale microprocessors have been presented in literature. These approaches utilize various techniques to distribute the clock signal across the chip with minimal clock skew and reasonable power consumption. Table 3.1 summarizes the various microprocessor architectures with respect to the technology, global clock geometry and worst case global skew.

Table 3.1. *Summary of electrical CDN reported in the literature.*

Microprocessor		Pentium 4	Pentium III	Itanium IA-64	S/390 G6	S/390 G5	Alpha 21364	Alpha 21264
Corporation	-	Intel	Intel	Intel	IBM	IBM	Compaq	Compaq
Channel length	nm	180	250	180	200	250	180	350
Frequency	MHz	2000	650	800	760	609	1200	600
Supply voltage	V	1.1-1.7	1.4-2.2	1.5	1.9	1.9	1.5	2.2
Die area	mm^2	217	140	464	215	212	397	318
Transistors	Mil	42.0	9.5	25.4	25.0	25.0	152.0	15.2
Metal layers	-	6	5	6	6	6	7	4
GCDN	-	binary	binary	H-tree	H-tree	H-tree	H-tree	Grid
Power per chip	W	75.3	~20	130	NA	25	150	72
Global Skew	ps	16	15	28	12	12	90	75
References	-	[KUR-01]	[SEN-99]	[TAM-00]	[AVE-99]	[AVE-99]	[XAN-01] [GRO-02]	[BAI-98]

3.4.1 The 21264 Alpha microprocessor.

The family of DEC/Compaq Alpha microprocessors represents significant milestones in high-speed microprocessor technology. Over the last years the clock frequency of the Alpha microprocessor has increased from 200MHz in 1992 [DOB-92] to 1.2GHz in 2001 [XAN-01]. The 21264, the third-generation of Alpha [BAI-98], is fabricated in a 0.35μm process and designed to operate at greater then 600MHz. The Alpha 21264 microprocessor is the first version of the Alpha family to utilize a hierarchy of clocks. A diagram of the clock hierarchy is presented in Fig.3.13. The clock hierarchy includes a gridded global clock, six gridded major clocks, and many local and conditional clocks.

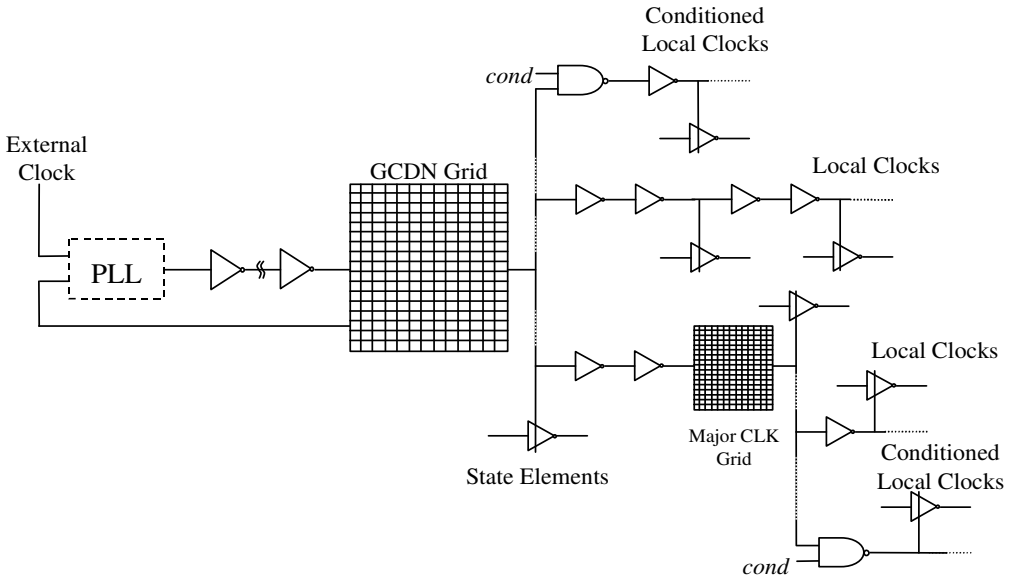
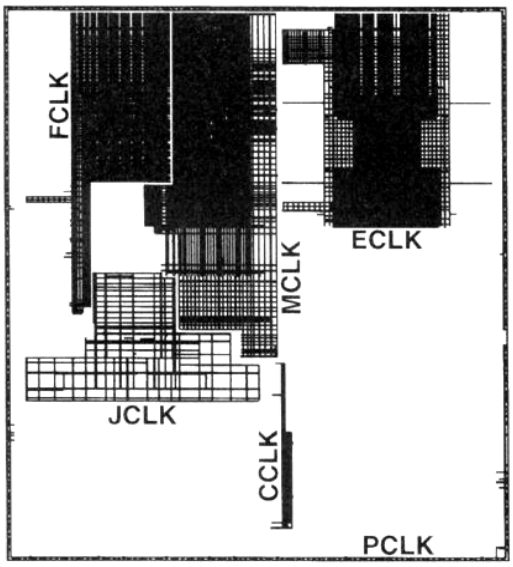


Fig.3.13. 21264 Alpha microprocessor clock hierarchy.

The clock generation is provided by an on-chip phase-locked loop (PLL). The global CDN grid traverses the entire die and uses 3% of upper level metallization. All interconnects within the GCLK grid are shielded both laterally and vertically by a power

and ground lines. In order to control phase alignment the GCDN is included in the feedback loop of PLL.



CCLK	Bus interface unit.
ECLK	Integer issue and execution units.
FCLK	Floating point issue and execution units.
JCLK	Instruction fetch and branch prediction unit.
MCLK	Load/store unit.
PCLK	Pad ring.

Fig.3.14. Major clock grid

In addition to the GCDN grid, there are six major regional clocks that drive large regional grids over their respective execution units as illustrated in Fig.3.14. The major clock grid density varies widely due to the wide variation of clock loads. The last part of the clocking hierarchy are the local clocks. In contrast to the GCDN grid and major clocks, local clocks are generally neither gridded nor shielded. There are no strict limits on the number, size, or logic function of local-clock buffers, however timing path constraints must always be met.

3.4.2 The IBM S/390 G5 microprocessor.

The IBM S/390 G5 microprocessor is fabricated on a 0.25μm, six-metal layer CMOS process, contains 25 million transistors, and is designed to operate at 609MHz [AVE-99]. The size of the G5 microprocessor is 14.6mm × 14.7mm, with 18 million

transistors for the array section and seven million for the logic section. The clock distribution hierarchy includes a global H-tree and local grid as is illustrated in Fig.3.15.

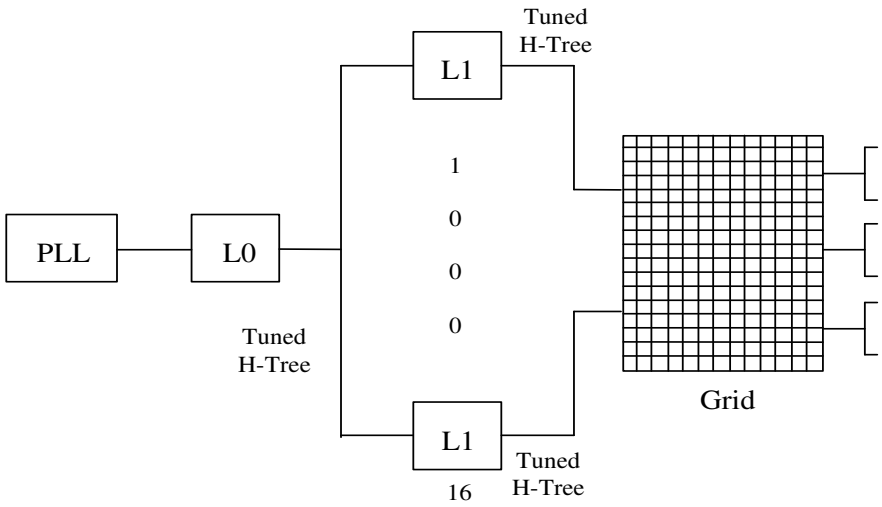


Fig.3.15. IBM S/390 G5 microprocessor clock hierarchy.

The clock generation is provided by a centrally located phase-locked loop that multiplies a slow external frequency by a factor of 8. A global H-tree distributes a low-skew clock signal from the central buffer to all 16 sector buffers as shown in Fig.3.16. The H-tree is placed on the top two metallization levels. Similarly to the Alpha microprocessor, each wire in the global H-tree is shielded by power and ground lines.

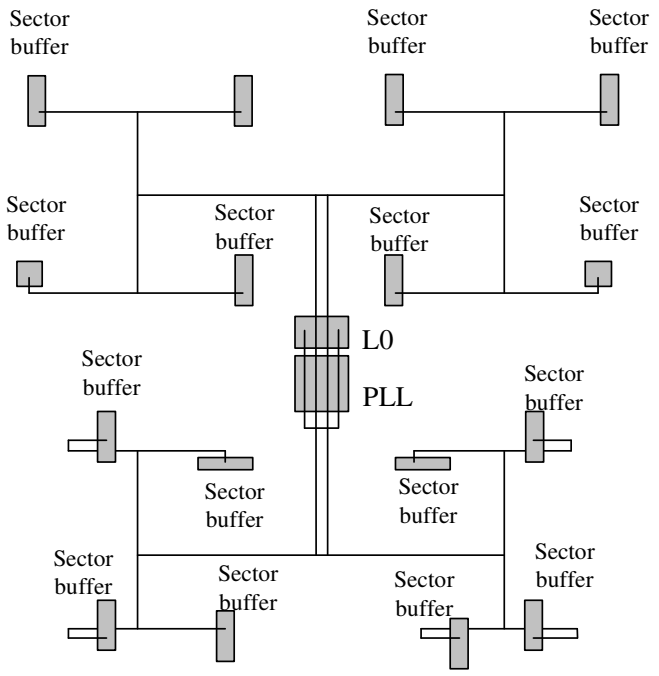


Fig.3.16. Global clock distribution H-tree.

Each sector buffer drives a second-level H-tree, which in turn drives the inter-section points of the clock grid. The grid consists of 32 horizontal wires and 32 vertical wires across the entire chip. Like the H-tree, the grid is shielded on both sides to reduce the coupling of noise into nearby signal wires. The grid connects all of the sectors into one common network.

3.4.3 The Intel IA-64 microprocessor.

The Itanium IA-64 is the first Intel implementation of a 64-bit microprocessor. The microprocessor core contains 25.4 million transistors placed on a 464mm^2 chip. IA-64 is fabricated in a 0.18μm, six-metal layer CMOS process, and operates at 800MHz. The architecture of the IA-64 clock distribution network consists of a three component global, regional and local distribution as shown in Fig.3.17.

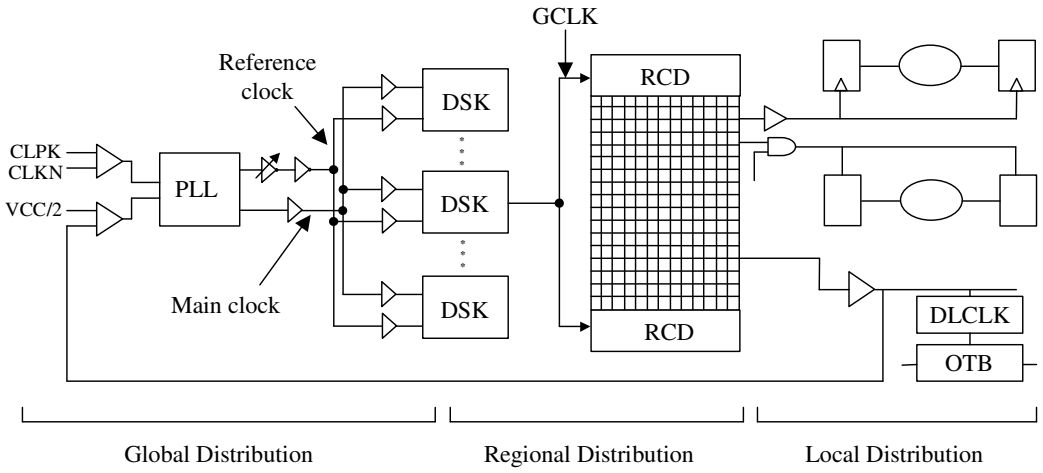


Fig.3.17. IA-64 clock distribution topology.

As with the previous approaches, the on-chip phase-locked loop is used to generate the clock signal. The H-tree global distribution network, which occupies the two highest-level metal layers, distributes the clock signal to the eight deskew buffers (DSK) as shown in Fig.3.18. In order to minimize the effects of any capacitive and inductive coupling between the clock lines and any adjacent signal lines, each wire of the global clock is fully shielded laterally by power and ground lines.

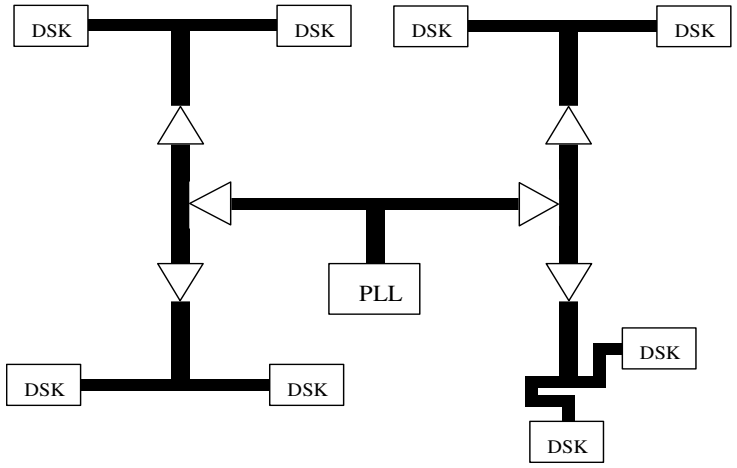


Fig.3.18. Schematic drawing of the global H-tree.

The regional clock distribution encompasses the DSK, the regional clock driver (RCD) and the regional clock grid. The regional clock distributes the clock signal to the 30 separate clock regions (regional clock grids). The regional clock grid is implemented using 4.1% of metal 4 (x-direction) and 3.5% of metal 5 (y-direction).

The local clock distribution constitutes the final segment of the clock distribution. It consists of the local clock buffers (LCBs) taking the input directly from the regional clock grid and the opportunity-time-borrowing (OTB) delay clock generation.

3.5 CLOCK SYSTEM SCALING

Signal integrity issues that occur with electrical interconnects for data transfer can cause extreme problems. This is particularly true for clock distribution networks (CDN) where sharp, well-timed clock edges are critical for overall performance of the system. As silicon circuits become more complex and clock rates increase, signal timing uncertainty becomes a greater problem. The need for an accurate clock can be a bottleneck in many applications.

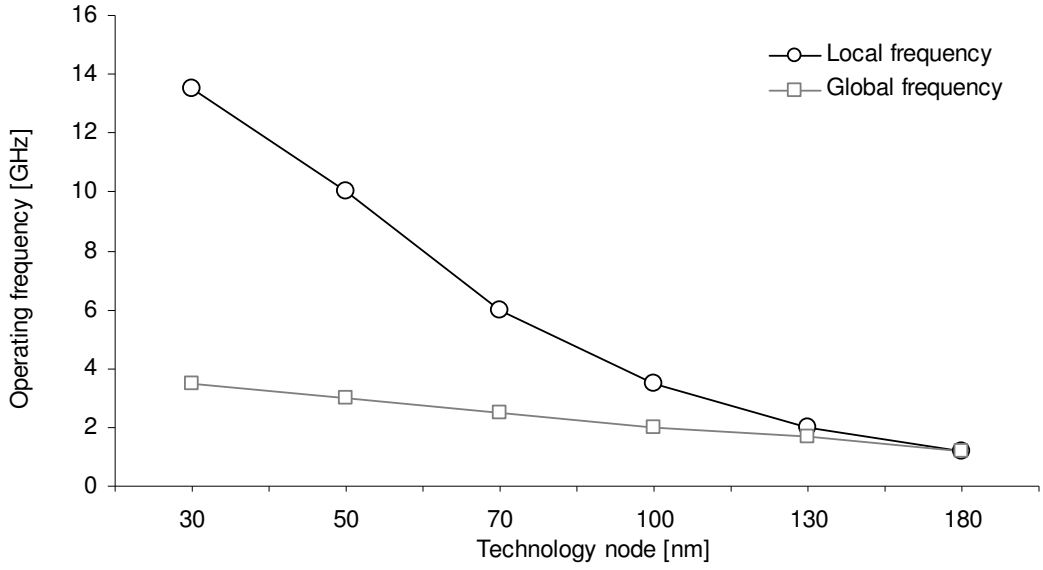


Fig.3.19. ITRS global and local clock frequency vs. technology generation.

Additionally, process variations in transistors and in wiring lead to skew that cannot easily be anticipated during layout. As the technology scales, the clock skew problem will get worse. Due to the bandwidth limitation of upper level interconnects, the low-skew global clock signal cannot be distributed at GHz frequency across the chip. One of the suggestions for coping with this difficulty is to separate the clock distribution network into a relatively slow global clock and fast local clocks. Fig.3.19. shows the ITRS prediction of clocking frequency in future integrated circuits. The difference between local frequency and the global frequency (frequency of signals travelling across the chip) tends to become progressively larger in the future due to the degradation of signal propagation delay caused by line-to-line and line-to-substrate capacitive coupling. To guarantee the high speed clock signal at the latches frequency multiplication circuits placed between the global and local clock network will be needed. However, this leads to higher power consumption and growth in circuit complexity. Is should be noted that as a solution to these problems, numerous researchers have proposed globally asynchronous locally synchronous (GALS) architectures [CHA-84, HEM-99, MEI-99, MUT-00, SJO-00]. A variety of GALS architectures have been proposed. The main idea assumes that the system is partitioned into smaller synchronous modules of logic which communicate with each other asynchronously. The communication between modules uses a well defined request acknowledge protocol. Since the synchronous modules are isolated from all other modules, different power supply voltage and clock speed are possible.

As the limits of electrical interconnects draw nearer, clocking will become even more problematic. Optical interconnections, which are a very attractive solution to solve on-chip global electrical interconnect problems can be also used in clock distribution systems. To overcome the need for clock multiplication circuits and thermal limitations of the electrical system we propose the replacement of the conventional global clock network by an optical H-tree.

3.6 CONCLUSION.

In this chapter an overview of clock distribution networks implemented within high-performance integrated circuits has been presented. The fundamental terminology and

concepts needed to understand synchronous systems have been introduced. The clock skew constraint relationship was presented as well as the main clock skew sources. The fundamental sources of the energy consumption in CMOS circuits have also been described. The most common present-day circuit strategies and topologies used to distribute the clock signal were discussed. First of all the buffered and symmetrical H-tree, which can be used to minimize clock skew within a chip, and thereby improves the circuit's overall performance. As an example various global clock distribution architectures and strategies used in several microprocessor chips were described.

IV. Modeling of Electrical Clock System

Chapter IV

Modeling of Electrical Clock System

4.1 INTRODUCTION.

Due to continually shrinking feature sizes, higher clock frequencies, and the simultaneous growth in complexity, the role of interconnections in determining circuit performance is growing in importance. This trend has led to the increasing dominance of interconnect delay over logic propagation delay – even with new metal technologies such as copper or new low-k dielectrics. The most recent microprocessors have as many as seven metal layers [KUR-01], [THE-00], while the ITRS predicts the use of up to 10 levels of wiring for the 45nm technology node in the year 2010 [ITRS-02]. High performance integrated circuits will count up to $2x10^9$ transistors per chip and work with clock frequencies up to 10 GHz.

Coping with the design of electrical interconnects under the above conditions is a formidable task [RAH-95], [HOR-99], [SAK-00], [YAM-00], [DAV-01] that requires adequate tools. Numerical simulation employing specially worked-out models allowing the evaluation of signal propagation in interconnect systems seems to fulfil this demand. Its application requires, however, appropriate models that can be employed in an electrical simulator such as SPICE. They can be created in different ways and a simple interconnect model corresponding VLSI technology, shown in Fig.4.1, will be used to demonstrate this.

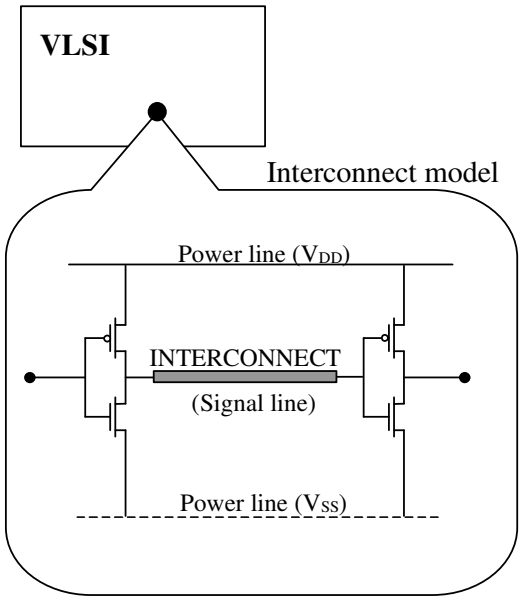


Fig.4.1. Interconnects in VLSI.

In general an interconnect system model on a VLSI chip covers two power lines and one signal line as shown in Fig.4.1. The technology used allows one to consider the power lines as a meshed network that plays the role of distributed current sources supplying all electronic elements equally. The signal line must, however, be considered as a transmission line coupling buffers sketched as CMOS inverters, and characterised by its resistivity, inductivity and capacivity. It can be modeled as an RC or RLC transmission line but in order to analyse the impact of interconnections on clock timing relationship and the power dissipated in the clock distribution system, it is necessary to calculate the parameters of lines associated with the system.

4.2 THE ICAL PERFORMANCE ESTIMATOR.

This chapter describes, the tool called "*Interconnect Calculator"* (ICAL) which allows one to model a global clock distribution network or single point to point electrical interconnects. This program provides designers with the capability to model, evaluate, predict and optimize global CDN networks for future technology nodes. ICAL explores the

effect of interconnect design and technology tradeoffs on IC performance. Default input data are extracted from the ITRS roadmap. Architecture requirements and the multilayer interconnect structure are taken into account. The core engine of ICAL combines a set of analytical models based on physical principles and empirical knowledge. These models, gathered from the published literature, encompass system architecture, circuit, interconnect and device characteristics which capture the essence of CMOS based microprocessor systems. The analytical models are grouped into several model units based on their subject, for example: interconnect unit, device unit, performance unit, power dissipation unit etc. The model and assumption used in each of these units are discussed in detail in subsequent sections. The flow diagram of the methodology used in ICAL is shown in Fig.4.2.

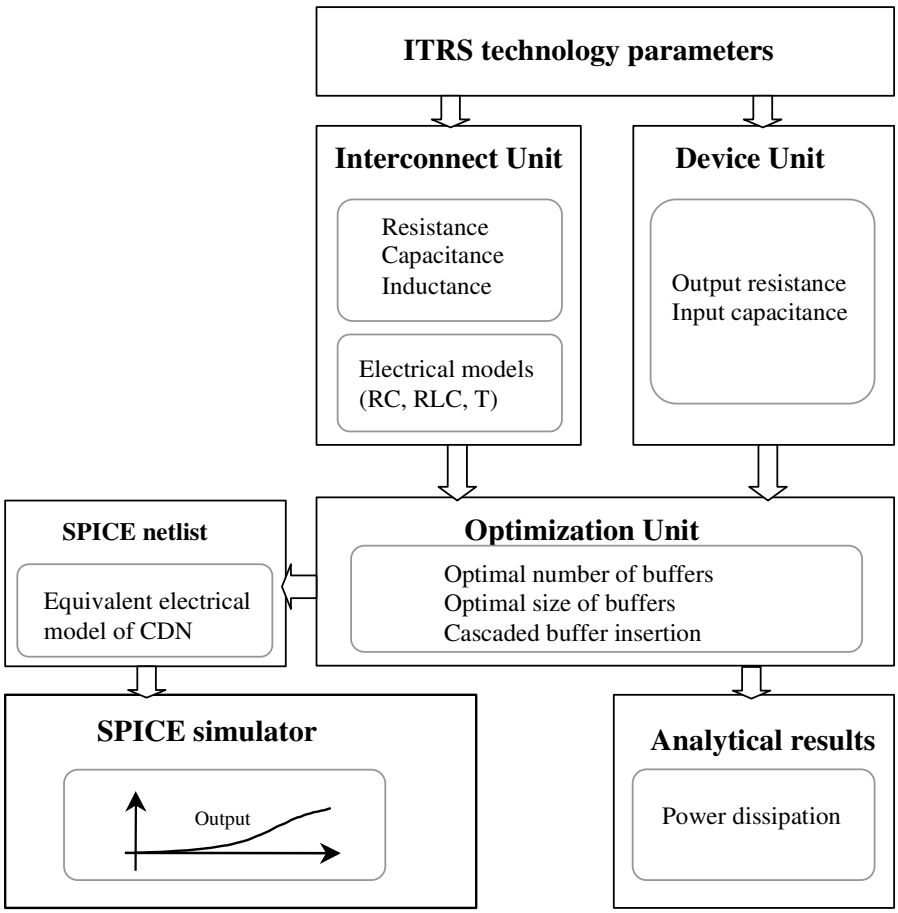


Fig.4.2. The flow diagram of the methodology used in ICAL software.

The first input to the ICAL program is the set of technology parameters for the process of interest, in particular the feature size, dielectric constant and metal resistivity according to the ITRS roadmap. In the next step, ICAL proceeds to calculate the resistance, capacitance and inductance for a given metal layer and the transistor parameters of minimum size inverters. Based on the parameters calculated previously, and the repeater insertion method, ICAL determines the optimal number and size of buffers needed to drive the clock network. For such system the program creates the SPICE netlist where the interconnect is replaced by RC or RLC distributed lines coupled by buffers designed as CMOS inverters. Berkeley BSIM3v3 and BSIM4 [BSIM] (see Appendix A) parameters were used to model the transistors used in the inverters. The clock timing relationship and the power dissipated in the system can be extracted from transistor-level simulations or directly from analytical equations.

The models and assumptions used in the ICAL program are discussed in more detail in the next sections.

4.3 INTERCONNECT UNIT

This section focuses on describing the interconnect issues in modern integrated circuits. The models used by ICAL to estimate accurately interconnect resistance, capacitance and inductance will be presented. The formulas presented below are used by ICAL to evaluate the impact of different interconnect structures and new technology materials on the clock system performance, such as power dissipation and propagation delay, which will be further described in the next sections.

4.3.1 Interconnect resistance.

As a result of downscaling of layout and technology rules, the influence of interconnects on the total feature of IC increases. The increasing parasitic resistance decreases the amplitude and increases the rise time of transmitted signals in signal

conductors and can also cause DC voltage drop in power distributing lines. It is desired, therefore, to minimize the interconnect resistance.

The interconnect resistance per unit length, R_o, is generally determined by following expression [BAK-85]:

$$R_o = \frac{\rho}{W*T} \tag{4.1}$$

where ρ is the resistivity of the metal layer, W is the width of the wire and T is its thickness. It must be, however, taken into account that the resistance can by change by skin effect occurring at high frequencies. If the frequency is sufficiently large, the electromagnetic field decay rapidly with depth inside of the conductor as it is shown in Fig.4.3.

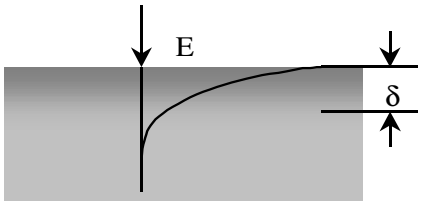


Fig.4.3. Skin effect in on-chip interconnect.

As result, the current flows near to the surface, which increase the resistance of the wire. The skin depth, δ, is given as [WHE-42]:

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}} \tag{4.2}$$

where f is the frequency, μ is the magnetic permeability of material and ρ is resistivity of the conductor. When the skin depth becomes less then the dimensions of the interconnection, the resistance increases and the skin effect must be considered. For copper at 1GHz, the skin depth is equal to 2.1μm.

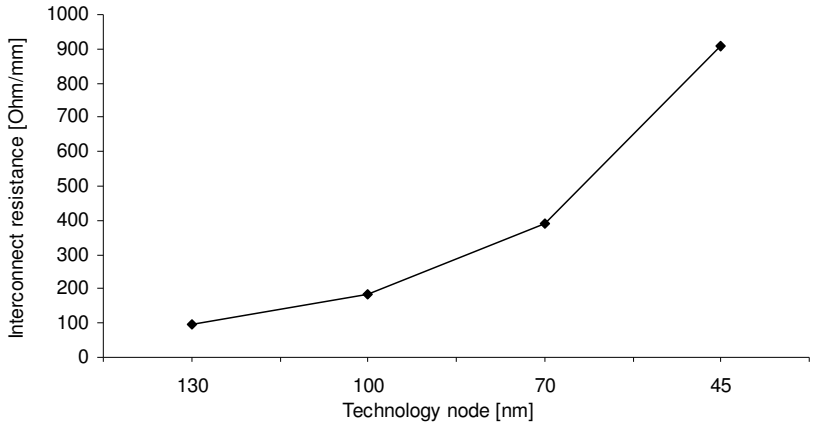


Fig.4.4. Global interconnect resistance versus technology generation.

Fig.4.4. shows the wiring resistance per unit length R_o calculated for global interconnect with minimum wire pitch as a function of technology nodes. It is clear from this figure that, as the cross-section dimensions of global interconnect shrink and operating frequency growths (skin effect) the parasitic resistance increases.

4.3.2 Interconnect capacitance.

Parasitic capacitances associated with the interconnections in the high density environment of the integrated circuit have become the primary factors in the evolution of the very high speed integrated circuit technology. Their evaluation is a non-trivial task and it is a subject of many investigations [RUE-75], [BER-88], [LEE-98]. An accurate model for the crossover capacitance is essential for estimating the interconnect circuit performance. To get an accurate interconnect capacitance electric field solvers (2D or 3D) should be used for the whole interconnect system [JEN-94], [CHE-96]. It is, however, so huge task that it would take ages for estimating capacitance of the whole chip. Therefore, various assumptions and approximations are used to get quick estimates. The simplest equation for interconnect capacitance is given by:

$$C = \varepsilon_o \varepsilon_{SiO2} \frac{W}{H} L_{Int} \tag{4.3}$$

where H is the interlayer dielectric (ILD) thickness, ε_{SiO2} is the relative permittivity of dielectric, ε_o is the permittivity of free space, W and L_{Int} are the width and length of the interconnect.

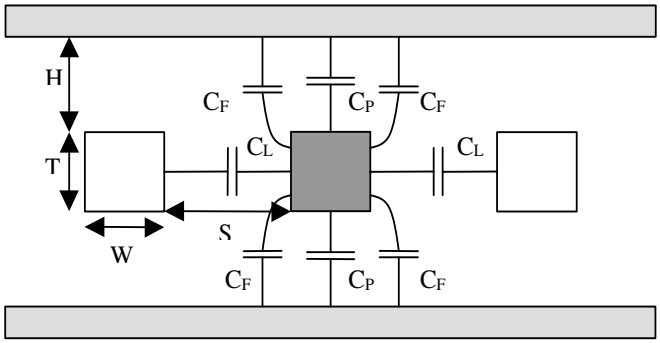


Fig.4.5. Interconnect capacitance components

For interconnect in modern integrated circuits a large part of the capacitance comes from lateral coupling between adjacent wires placed on the same metal level and from fringing fields This means that the values of extracted capacitance using simple parallel plate capacitor approximations are extremely inaccurate. In reality, the total interconnect capacitance is a sum of a few different capacitances resulting from the particular design of interconnect system and cannot be treated as the simple plane described by (4.3). As it is shown in Fig.4.5, one can distinguish the parallel plate capacitance component, C_P, the fringing field component, C_F, and lateral coupling capacitance component, C_L. It should be noted, that if the neighbor line is switching in the opposite direction, the effective lateral capacitances doubles but if the neighbor line is switching in the same direction the effective lateral capacitances is equal zero.

There are several approaches to identify the total capacitance C_{Total}, which use different models to define the components capacitances The most popular of them will be presented below. One of the first one was developed by Sarasvat [SAR-82]. He considered the structure shown in Fig.4.5 and described the component capacitances as follows:

$$C_P = \varepsilon_{ox}\varepsilon_o \frac{W}{H} \tag{4.4}$$

$$C_L = \varepsilon_{ox}\varepsilon_o \frac{T}{S} \tag{4.5}$$

$$C_{Total} = k(2C_P + 2C_L) \tag{4.6}$$

where T - line thickness, S - distance between two adjacent wires and k - the factor which takes into account the fringing fields, which value can be calculated using two-dimensional analysis of Dang and Shigyo [DAN-81].

Another model was presented by Sakurai [SAK-83] who derived a simple analytical formula for the total capacitance for symmetrical interlevel dielectric thickness. However, this formula takes into account a basic wire structure with one ground plane only. Because of the symmetrical nature of the interconnect structure considered in this work, like is shown in Fig.4.5 the capacitance between wire and ground $C_{vertical}$ and capacitance between adjustment wires $C_{horizontal}$ are multiplied by two.

$$C_{vertical} = \varepsilon(1.15(\frac{W}{H}) + 2.80\,(\frac{T}{H})^{0.222}) \tag{4.7}$$

$$C_{horizontal} = \varepsilon(0.03(\frac{W}{H}) + 0.83\,(\frac{T}{H}) - 0.07\,(\frac{T}{H})^{0.222})(\frac{S}{H})^{-1.34}) \tag{4.8}$$

$$C_{Total} = 2C_{vertical} + 2C_{horizontal} \tag{4.9}$$

Chern in [CHER-92] presented more complex crossover model for triple-level metal layer, which were the base for the below formulas:

$$C_{vertical} = \varepsilon(\frac{W}{H} + 1.086\,(1 + 0.685e^{\frac{-T}{1.343S}} - 0.9964\,e^{\frac{-S}{1.421H}})(\frac{S}{S+2H})^{0.0476}(\frac{T}{H})^{0.337}) \tag{4.10}$$

$$C_{horizontal} = \varepsilon\left(\frac{T}{S}\left(1-1.897e^{\frac{-H}{0.31S}}\right)^{\frac{-T}{2.474S}} + 1.302\, e^{\frac{-H}{0.082S}} - 0.1292e^{\frac{-T}{1.421S}}\right) \quad (4.11)$$

$$+1.722\left(1-0.6548e^{\frac{-W}{0.3477H}}\right)e^{\frac{-S}{0651H}}$$

$$C_{Total} = 2C_{vertical} + 2C_{horizontal} \quad (4.12)$$

The last formula that will be presented here is taken from Wong work [WON-00]. According to his model, the interconnect capacitance is described as:

$$C_{vertical} = \varepsilon\left(\frac{W}{H} + 2.217\left(\frac{S}{S+0702H}\right)^{2.193} + 1.17\left(\frac{S}{S+1.510H}\right)^{0.7642}\left(\frac{T}{T+4.532H}\right)^{0.1204}\right) \quad (4.13)$$

$$C_{horizontal} = \varepsilon\left(1.412\frac{T}{S}\exp\left(\frac{-4S}{S+8.014H}\right) + 2.3704\left(\frac{W}{W+0.3078S}\right)^{0.25724}\right. \quad (4.14)$$

$$\left.\left(\frac{H}{H+8.961S}\right)^{0.7571}\exp\left(\frac{-2S}{S+6H}\right)\right)$$

$$C_{Total} = 2C_{vertical} + 2C_{horizontal} \quad (4.15)$$

In order to recognize which one from the above formulas gives the evaluation of the total capacitance that suits to the real capacitance of the interconnect line, the numerical simulations based on the numerical solving of Maxwell equations have been employed. The simulations were performed using the commercial software package OPERA [VEC], which uses finite element techniques to analyze the electromagnetic problems. The test interconnect structure is shown schematically in Fig.4.6. It contains of three wires sandwiched between a two ground planes.

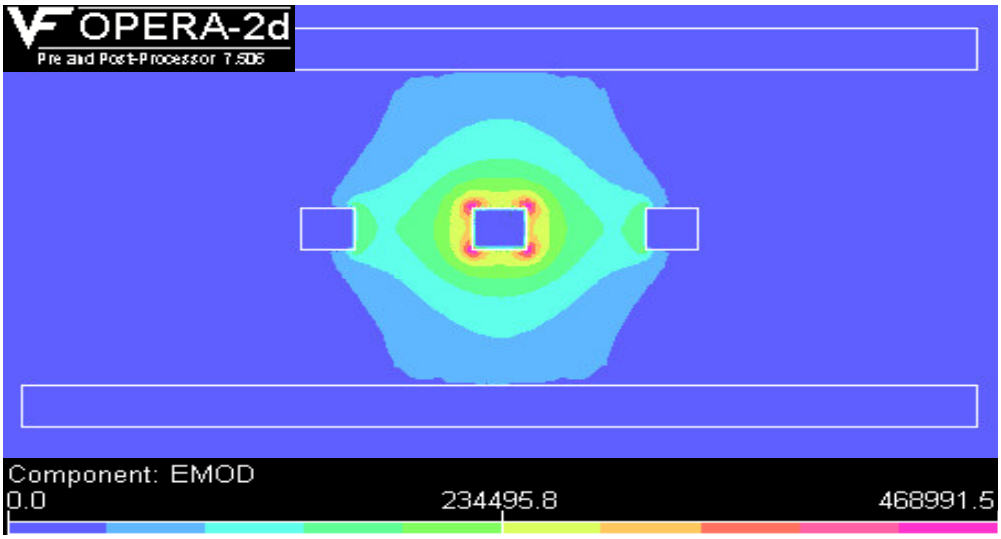


Fig.4.6. Interconnect structure used in numerical capacitance calculation.

The total capacitance was calculated numerically and using four mentioned above formulas. Such a procedure has been repeated for several structures fabricated in 0.13, 0.10 and 0.05 μm CMOS process, which design parameters are collected in Table 4.1.

Table 4.1. *Cross-section interconnect dimensions.*

Technology	Layer	w	t	s	h	Eps	V
		[m]	[m]	[m]	[m]	-	[V]
130	1	1.46E-07	1.08E-07	1.54E-07	3.55E-07	2.00	1.20
	6	2.35E-06	2.00E-06	2.53E-06	6.67E-06	2.00	1.20
100	4	1.18E-07	2.04E-07	1.22E-07	3.55E-07	1.50	0.90
	7	2.22E-06	2.00E-06	4.98E-06	6.67E-06	1.50	0.90
50	7	1.20E-06	1.50E-06	1.20E-06	9.00E-07	1.50	0.60
	9	2.00E-06	2.50E-06	2.00E-06	1.40E-06	1.50	0.60

Eps – dielectric constant

The discrepancies between the total capacitance evaluation by means of analytical formulas and the OPERA simulations are shown in Table 4.2. The error used as the discrepancy measure is defined as follow:

$$\text{Error} = \frac{\text{Analytical calculation - Numerical calculation}}{\text{Numerical calculation}} 100\%. \quad (4.16)$$

Table 4.2. *Error table of the analytical formulas compared with numerical simulator.*

Tech.	Layer	OPERA	[CHER-92]	error	[WON-00]	error	[SAK-83]	error	[SAR-82]	error
130	1	7.36E-14	7.84E-14	7%	8.26E-14	12%	1.16E-13	58%	3.94E-14	-46%
	6	7.39E-14	7.88E-14	7%	8.46E-14	14%	1.17E-13	58%	4.05E-14	-45%
100	4	7.63E-14	8.07E-14	6%	9.19E-14	20%	1.23E-13	61%	5.32E-14	-30%
	7	4.37E-14	4.56E-14	4%	5.23E-14	20%	7.51E-14	72%	1.95E-14	-55%
50	7	8.61E-14	9.22E-14	7%	1.06E-13	23%	1.48E-13	72%	6.86E-14	-20%
	9	8.93E-14	9.39E-14	5%	1.09E-13	22%	1.52E-13	70%	7.11E-14	-20%

Based on this comparison one can judge that the empirical Chern's formula that error value is less then 8% over a wide range of interconnect parameters can be trated as the more realistic. This formula is set as default in ICAL program, however it is possible to choose other formulas. It should be noted that the valid range of interconnect dimensions for this formula is [CHER-92].

$$0.3 \le \frac{W}{H} \ge 10; \qquad 0.3 \le \frac{H}{T} \ge 10 \quad (4.17)$$

Fig.4.7. shows the wiring capacitance per unit length C_o calculated by Chern's formula as a function of technology nodes. The calculations have been done for global interconnect with minimum cross-section dimensions (minimum wire pitch). It can be notice that the interconnect capacitance calculated for the present value of dielectric constant 3.6 remain almost the same, while the capacitance calculated for the values predicted by ITRS tends to lessen.

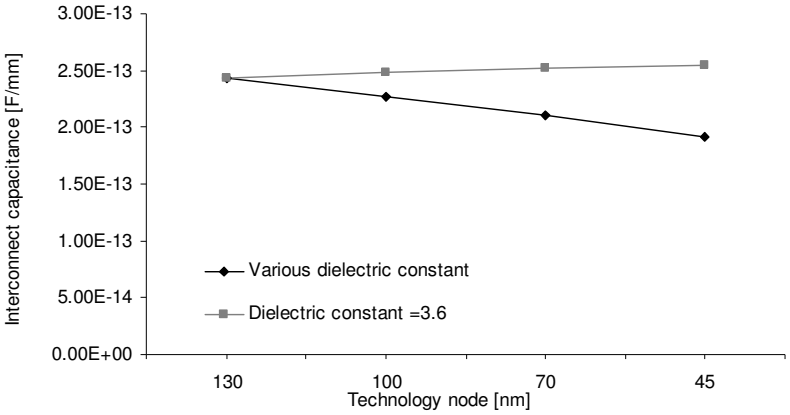


Fig.4.7. Global interconnect capacitance versus technology generation.

4.3.3 Interconnect inductance.

In today's VLSI circuits, the inductance starts to become significant due to longer metal interconnections, reduction in wire resistance (as a result of copper application and wider upper-layer lines) and higher frequency operations [DEU-95, DEU-97, KRA-98, ISM-99, ISM-00]. This is especially true for the global interconnect lines such as those in clock distribution networks, where the delay and the slope of clock waveforms are critical to overall system performance.

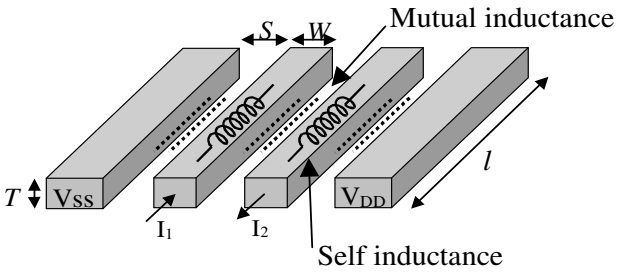


Fig.4.8. On-chip interconnect inductance.

On-chip inductance has significant impact on delay variations, degradation of signal integrity due to overshoots/oscillations, crosstalk, and increased power grid noise.

Accurate analysis of inductance is therefore critical for predicting the performance of interconnects, which in turn are crucial for determining the chip performance. The accuracy of the inductance analysis is also important for the precise quantification of their impact on performance optimization. The main difficulty in the extraction of on-chip inductance is the fact that the inductance is a function of a closed current loop. To extract accurately the on-chip inductance it is necessary to determine the return paths of the current. In addition, these return paths are different for DC and AC signals. Hence, precise inductance values cannot be calculated without the detailed information, such as location of the clock lines and neighboring wires. Under some assumptions, however, such as uniform current distribution, there exist closed form expressions for partial self and mutual inductances for certain types of geometries. For a rectangular conductor shown in Fig.4.8. the partial self inductance is given by [GRO-45]:

$$L=\frac{\mu_o l}{2\pi}\left[\ln\left(\frac{2l}{W+T}\right)+0.5+\frac{0.2235(W+T)}{l}\right] \tag{4.18}$$

where μ_o is the magnetic permeability, W is the width, T is the thickness, and l is the length of the conductor. Similarly, the mutual inductance between two equal length parallel conductors is given by:

$$M=\frac{\mu_o l}{2\pi}\left[\ln\left(\frac{2l}{S}\right)-1+\frac{S}{l}\right] \tag{4.19}$$

where S is the distance between the two metal wires.

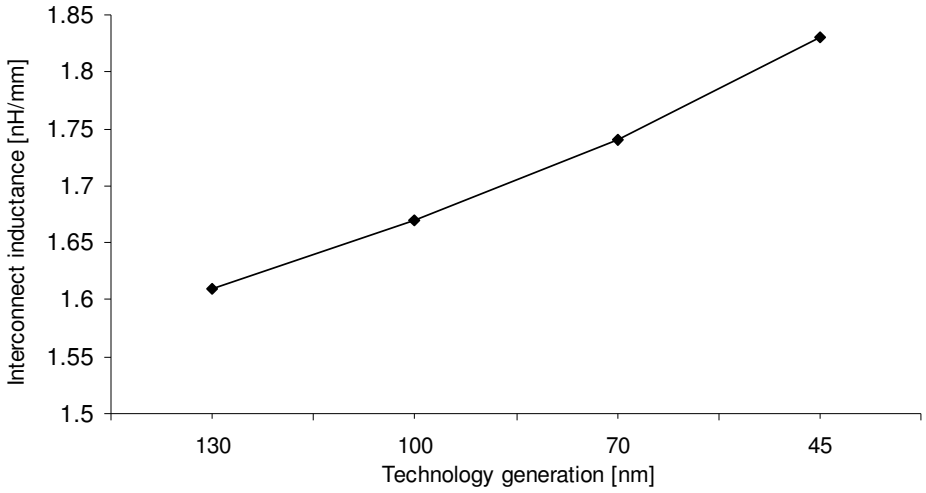


Fig.4.9. Global interconnect inductance versus technology generation.

Fig.4.9. shows the ICAL calculation of the wiring inductance per unit length L_o proceeded for global interconnect with minimum wiring pitch as a function of various technology nodes.

4.3.4 Electrical models of interconnect used by ICAL.

Initially, interconnection has been modelled as a single lumped capacitance in the analysis of the performance of on-chip interconnects. Next, with the scaling of technology and increased chip size the resistance of interconnection has been taken into account. The on-chip wires have become modeled as a lumped RC circuits [RUB-83]. Fig.4.10. illustrates different types of such a lumped RC circuit. There are L, Π and T section according to the shape of their unit block. The chose of the circuit must be restricted because it does not reproduce the correct response when the line is driven bidirectionally. Sakurai [SAK-83] shows that the L-section model is a poor approximation with relative error of delay amount to as much as 30%, while Π and T models presents the relative error of delay less then 3%. The accuracy of Π and T models is similar, however the computational time in circuit simulators is smaller when the Π-section model is used. This is because the T network has one node more then Π-network.

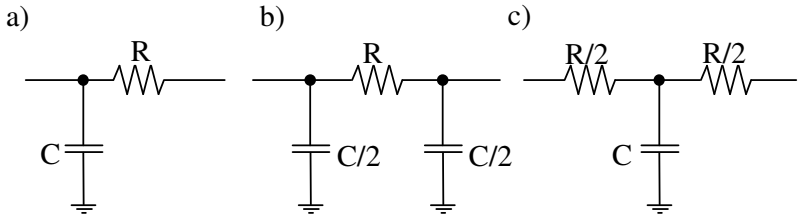


Fig.4.10. Lumped circuit used to approximate a wiring, a) L-section, b) Π-section, c) T-section.

The lumped RC models are completely sufficient for the interconnects that are short compared to wavelength. One should, however, remember that the parasitics components like the capacitance and resistance are not lumped into a single position, but are distributed along the wire. A schematic representation of a distributed RC line is shown in Fig.4.11.a).

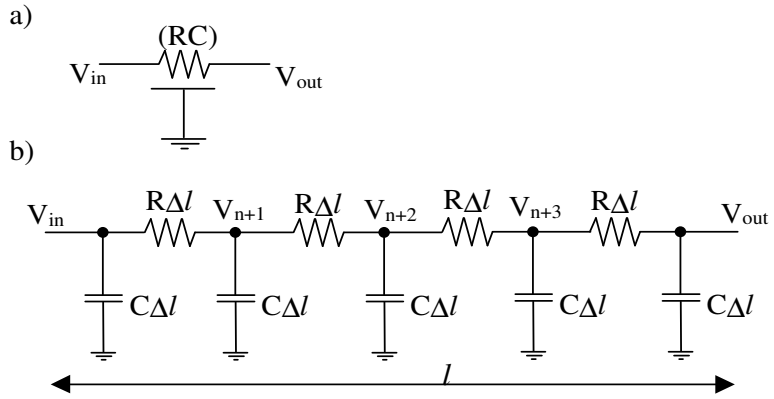


Fig.4.11. Basic topology of distributed RC interconnect model. a) Schematic symbol. b) Distributed model.

The voltage drop in such a long line is described by the well known differential equation that is in form:

$$RC\frac{\delta V}{\delta t}(x,t) = \frac{\delta^2 V}{\delta x^2}(x,t) \tag{4.20}$$

where V is the voltage at a particular point along the wire, and x is a distance between this point and the signal source. This equation is called the diffusion equation and has no closed-form solution. It is known, however, that the distributed nature of the wire allows approximating its features by considering the wire as divided into n smaller lumped section as is shown in Fig.4.11.b). The approximation accuracy increases of course with increasing number of sections (n).

Currently, inductance becomes more and more important with faster on-chip rise times and longer wire lengths. Wide long wires are frequently encountered in clock distribution networks. These wires are low resistive lines that can exhibit significant inductive effects. The presence of inductance in wire introduces ringing and overshoot phenomena not occurred in RC circuits. In such cases, the inductance cannot be omitted and the RLC nature of the transmission lines must be taken into consideration. The simple diffusion approach represented by (4.20) cannot be longer used and the partial differential equation (4.21) well-known as the propagation equation that describes a distributed RLC line must be considered.

$$\frac{\delta^2 V}{\delta x^2}(x,t) = RC\frac{\delta V}{\delta t}(x,t) + LC\frac{\delta^2 V}{\delta t^2}(x,t) \tag{4.21}$$

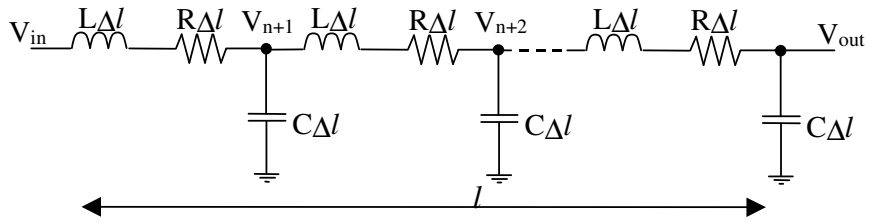


Fig.4.12. Distributed RLC interconnect model.

While in a distributed RC line signal diffuses from source to the destination according to the diffusion law In a distributed RLC line, signal propagates over the interconnection media with the speed defined as:

$$\upsilon = \frac{l}{\sqrt{LC}} = \frac{c_o}{\sqrt{\varepsilon\mu}} \tag{4.22}$$

where c_o is speed of light in vacuum, ε is the dielectric constant and μ is magnetic permeability. Similar as in the case of RC line, the distributed RLC line can be approximated by *n* section of lumped RLC elements as shown in Fig.4.12 [DAV-99], [DAV-00].

The effect of inductance must be taken into account when the interconnect length is long enough for the time of flight be comparable with rise time, T_{Rise} and is short enough such the attenuation does not eliminate the inductive effects. This two figure of merit are combined in equation:

$$\frac{T_{Rise}}{2\sqrt{LC}} < \text{Wire length} < \frac{2}{R}\sqrt{\frac{L}{C}} \tag{4.23}$$

This condition determines the range of the interconnection length within the inductance is important, so RC model is not sufficient. The range depends on the *R*, *L*, *C* parameters of the interconnection per unit length and on the transition time of the input signal.

Depending on considered circuit, the ICAL program allows the using of the RC, RLC lumped and distributed models (with any number of cells) and the SPICE lossy transmission line model. However, the RLC distributed model is set as default.

4.3.5 Equivalent electrical model of symmetrical H-tree.

In order to create the SPICE netlist, ICAL use the electrical models of interconnect described previously, which are coupled by buffers designed as CMOS inverters. In the

case of distributed RC and RLC lines, the number of cells is set to be as large as possible to increase the accuracy of the simulations. Along with the several levels of H-tree used in clock distribution system this can leads to the large complexity of the electrical system, which further increase the simulation time. In order to decrease the SPICE simulation time it is necessary to create an equivalent circuit of symmetrical H-tree.

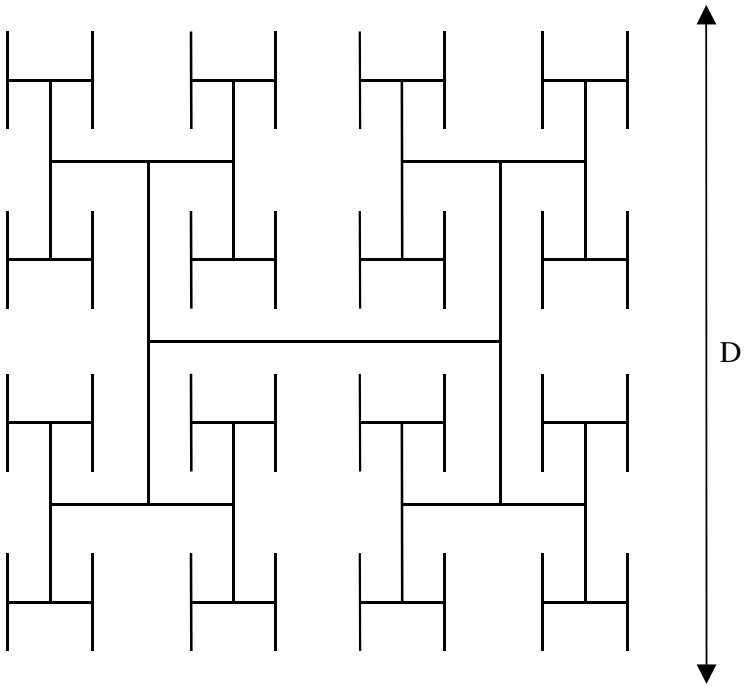


Fig.4.13. The 64 output nodes symmetrical H-tree.

The symmetrical H-tree clock distribution system with N nodes distributed regularly on an $D \times D$ die is shown in Fig.4.13. As the H-tree is symmetric, nodes at equal levels can be shorted together. It reduces the analysis to that of the interconnect circuit shown in Fig.4.14.b) and equivalent buffer circuit shown in Fig.4.14.c)

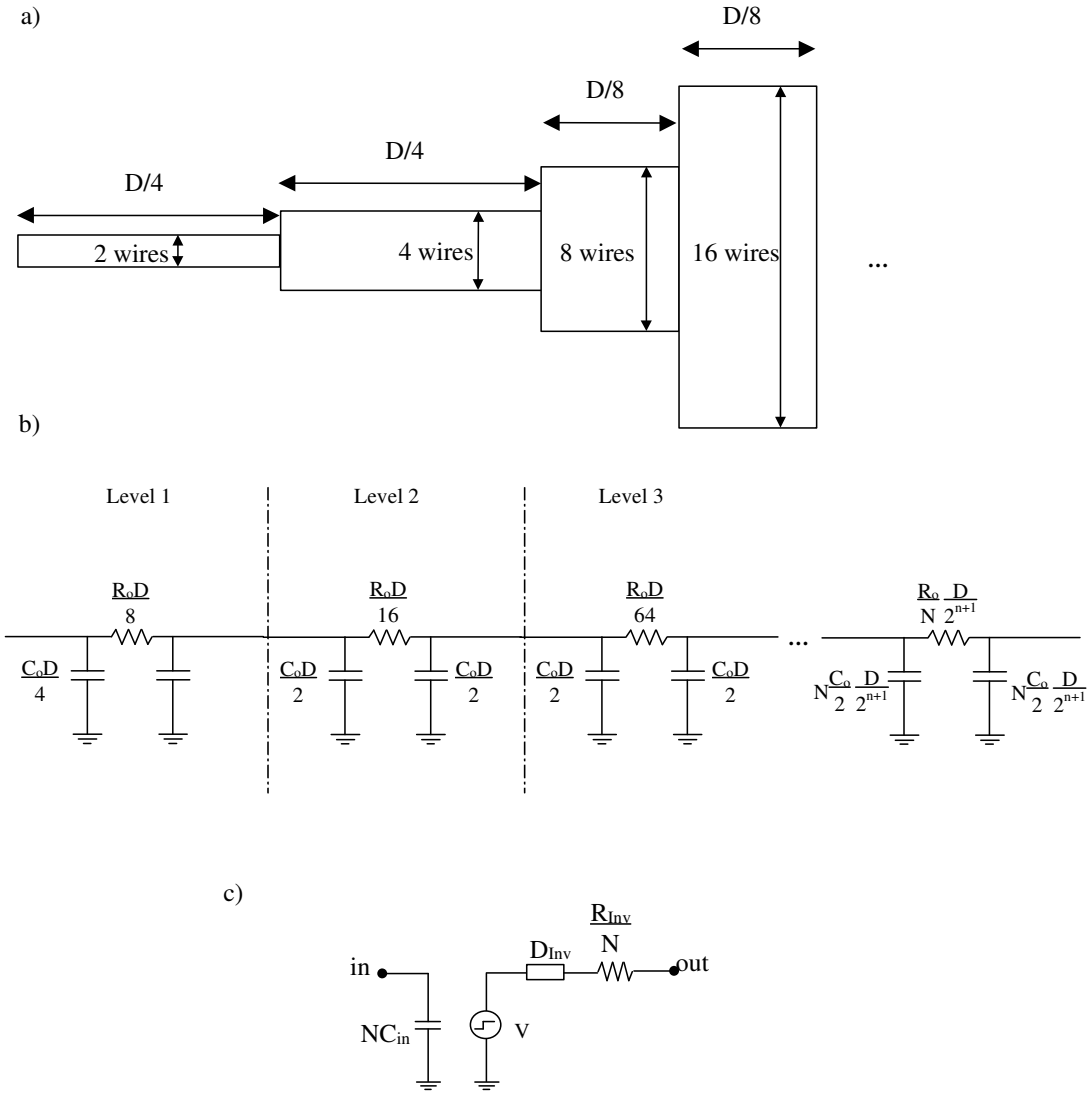


Fig.4.14. The equivalent circuit of the system components used in a symmetrical H-tree. a) Schematic diagram of wires in H-tree network. b) RC equivalent interconnects circuit. c) Equivalent buffer circuits.

In the example shown in Fig.4.14. the circuit consists of several RC lines separated by buffers. Each 'H' of the H-tree is replaced by two levels of RC segments using a equivalent π-model . Level 1 in Fig.4.14.a) corresponds to two branches of the tree, level 2 to four branches, etc. The arms of any H structure are of equal length, its value double from one H-level to the next. For an *n* number of H-tree used in the system the interconnect resistance and capacitance in the π-model can be described as:

$$R = \frac{R_o}{N}\frac{D}{2^{n+1}} \tag{4.24}$$

$$C = N\frac{C_o}{2}\frac{D}{2^{n+1}} \tag{4.25}$$

where R_o and C_o are the interconnect resistance and capacitance per unit length, respectively, N is number of output nodes (arms) in last level of H-tree and D is die width. The last term in these equation ($D/2^{n+1}$) express the length of the H arms in the last H-tree.

4.4 DEVICE UNIT.

As is described in Chapter 2 the most popular method for distributing clock signals in VLSI applications is to insert buffers at the clock source and/or along a clock path, forming a tree structure. Although interconnect delay becomes dominant in VLSI systems, it is still very important to take into account the impact of logic devices (buffers) used in the system. The switching speed of CMOS inverters used as buffers is basically a function of RC time constants. A typical on-chip interconnection consists of a CMOS inverter driving another CMOS inverter by distributed RLC wire as shown in Fig.4.15.a).

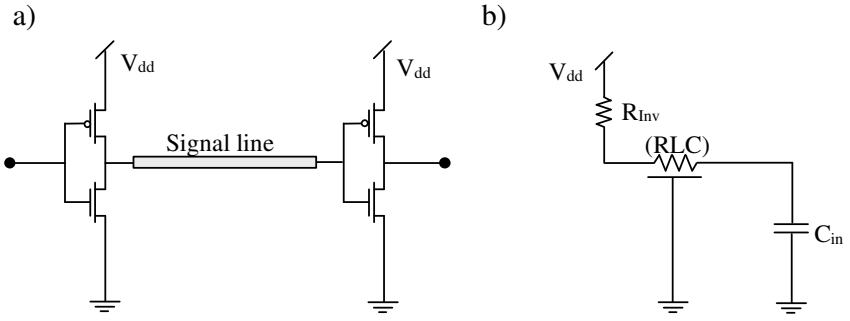


Fig.4.15. CMOS inverter driving another CMOS inverter by distributed RLC wire. a) general interconnection circuit, b) equivalent model.

This structure can by approximated by a simple RLC model shown in Fig.4.15.b). Here, the distributed RLC wire is connected to the output resistance R_{Inv} of the first inverter and to the input capacitance C_{in} of the second one. Accurate characterization of the MOSFET transistor is crucial for any high speed digital integrated circuit analysis and design. There are numerous references that develop the details of the physics of MOS device operation [YAN-99], [VEE-00]. In order to calculate the clock path delay, buffers incorporated into ICAL program are modeled by an equivalent circuit shown in Fig.4.16.a) and by the transistor level model shown in Fig.4.16.b). Where D_{Inv} is the buffer internal delay R_{Inv} is the buffer output resistance, C_{in} is the buffer input capacitance and V is the logic swing on the clock lines. In order to achieve small delay time the buffer driving resistance and input capacitance are designed to have small values. In the transistor level model the Berkeley BSIM3v3 and BSIM4 parameters were used.

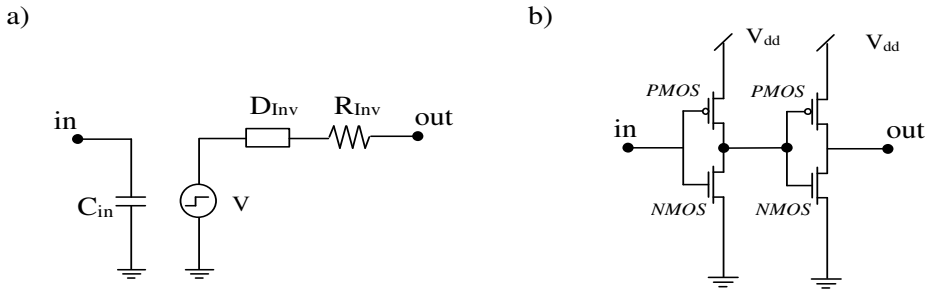


Fig.4.16. Models of buffer devices. a) Equivalent circuits. b) Transistor level model.

4.4.1 Device resistance.

The resistance of MOSFET transistors operating as switches is affected by several parameters. Fig.4.17. shows the various resistive components of MOSFET device. The largest resistive component is the channel resistance R_{Ch}, determined by the effective W_t/L_t ratio and the access bias. For majority of transistor switch layouts, the most important parasitics series resistance are R_c – contact resistance, R_{sh} – drain (and source) layer sheet resistance, R_{ac} – accumulation resistance, R_{sp} – spreading resistance [NG-87],

[THO-98], [CHO-00]. Two last components are associated with drain (and source) extension region.

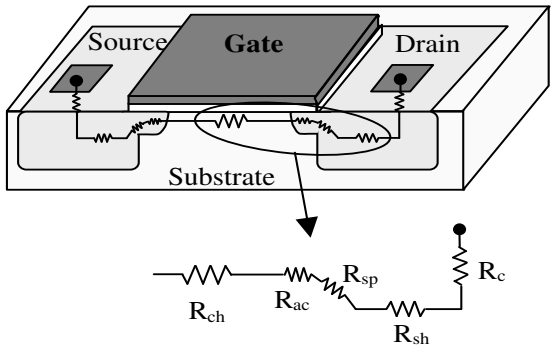


Fig.4.17. Components of MOSFET parasitic resistance.

The transistor output resistance R_{tr}, can be approximated by the sum of channel and parasitic source and drain contact resistances. The value of source and drain contact resistance is usually the same what allows presenting the output resistance as:

$$R_{tr} = R_{Ch}+2R_c \tag{4.26}$$

The value of channel resistance R_{Ch} fluctuates with the voltage level and with the temperature. An approximate estimation of the transistor channel resistance can be obtained from [VEE-00]:

$$R_{Ch} \approx \frac{L_t/W_t}{\mu C_{OX}(V_{DD}-V_T)} \tag{4.27}$$

where μ is the channel mobility, V_{DD} is the power supply voltage, V_T is the threshold voltage and C_{OX} is the oxide capacitance per unit area. Equation (4.27) is derived from the large signal I-V equations of MOSFET operating in the saturation region close to the linear region and is accurate for small channel geometries.

Contact resistance R_c is a measure of the ease with current can flow across a metal-semiconductor interface. Since aggressive scaling of IC devices has resulted in smaller

contact sizes and higher current densities, the contact resistance between the silicide and doped Si source/drain regions becomes constitutes a significant fraction of the parasitic series resistance in the path of the drain current. The metal-semiconductor contact resistance R_c, of a MOS device is given by:

$$R_c = \frac{\rho_c}{A_{contact}} \tag{4.28}$$

where $A_{contact}$ is the area of the contact window, ρ_c is the specified material contact resistivity

The inverter effective output resistance depends on transconductance of the pull-up or pull-down transistors. The NMOS resistance is used for a low to high input transition and the PMOS resistance is used for a high to low input transition. In general, the inverter effective output resistance may be approximated as the parallel combination of NMOS and PMOS transistors output resistances. For a minimum size inverter, the effective output resistance is given by:

$$R_{INV} = \frac{1}{2}\left(R_{NMOS} + \frac{R_{PMOS}}{2}\right) \tag{4.29}$$

Since the PMOS transistor is usually two times wider then NMOS transistor, the effective PMOS resistance is halved in the equation (4.29).

4.4.2 Device capacitance.

Fig.4.18. shows the major components of the transistor parasitic capacitance. The values of parasitic capacitance influence intensively the device characteristics in the short channel region [HOL-02]. Therefore, accurate models of the parasitic device capacitance are needed. This paragraph presents the simple analytical formulas used by ICAL to estimate the transistor parasitic capacitances.

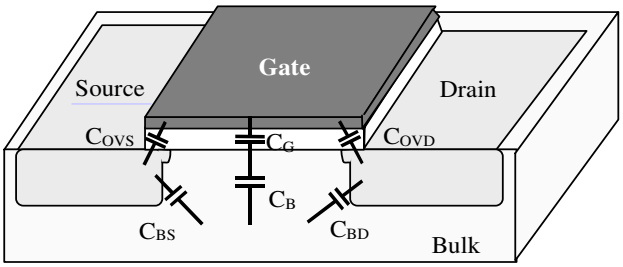


Fig.4.18. Different capacitance components in MOS structure.

Junction capacitances

The junction capacitances, C_{BD} and C_{BS} are associated with the back-biased depletion region between the drain and substrate and the source and substrate. The depletion-region capacitances are nonlinear and decreases when the reverse bias is raised. The junction capacitances, C_{BD} and C_{BS}, consist two parts: bottom-plate and side-wall, both have different physical characteristics. The bottom-plate junction is formed by the source and the substrate region, and for the source region is described by:

$$C_{bottom\text{-}plate} = Cj\ A_S \left[1-\frac{V_{BS}}{PB}\right]^{-Mj} \tag{4.30}$$

where, Cj, is zero-bias junction capacitance (per unit area), A_S, is area of the source region, V_{BS}, is voltage across the junction, PB, is the bulk junction potential and Mj is bulk-junction grading coefficient. The side-wall junction is formed by the source and the channel-implant region and for the source region is described by:

$$C_{side\text{-}wall} = Cjsw\ P_S \left[1-\frac{V_{BS}}{PB}\right]^{-Mjsw} \tag{4.31}$$

where, Cjsw, is zero-bias bulk-source side-wall capacitance, P_S, is perimeter of source region and Mjsw is bulk-drain side-wall grading coefficient. The total junction capacitances, C_{BS} (or C_{BD}) is the sum of bottom-plate and side-wall capacitances:

$$C_{BS} = C_{bottom\text{-}plate} + C_{side\text{-}wall} \tag{4.32}$$

A closer examination of the depletion capacitors is shown in Fig.4.19. According to this figure, the area of the drain region A_D, and the perimeter of drain region P_D are given by:

$$A_D = W\, L_D\ ; \qquad P_D = W+2L_D \tag{4.33}$$

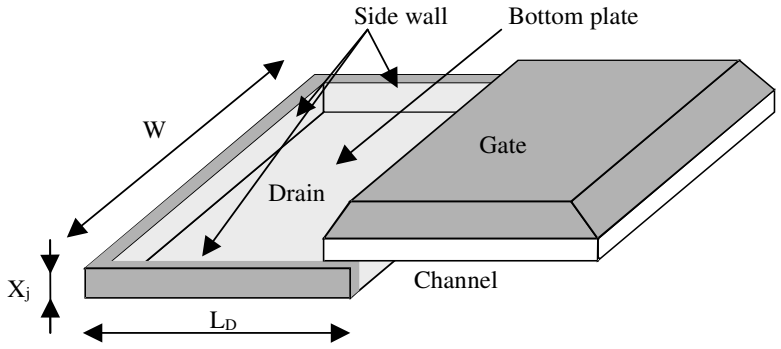


Fig.4.19. Detailed view of drain junction.

Gate capacitance.

The gate capacitance is split into: the constant overlap capacitances C_{OVD} , C_{OVS} , and C_{OVGB} and the variable capacitances C_{GS}, C_{GD}, and C_{GB}, which depend on the operating region. The constant overlap capacitances C_{OVD} and C_{OVS} are due to an overlap of two conducting surfaces separated by a dielectric. C_{OVGB} occurs between the gate and bulk at the edges of the channel and is a function of effective channel length. The overlapping capacitors are shown in more details in Fig.4.20.

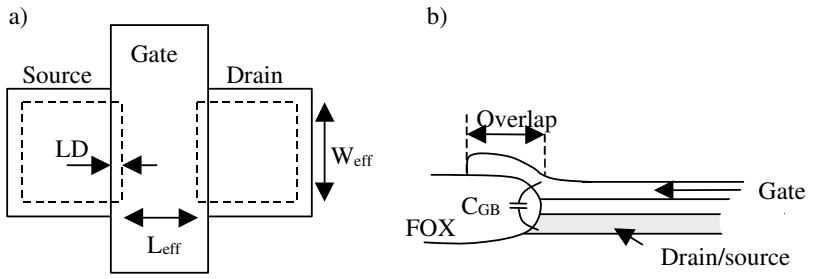


Fig.4.20. Overlap capacitances of an MOS transistor. a) Top view of overlap between source or drain and gate. b) Overlap between gate and bulk.

The amount of overlap is designated as LD. The overlap capacitances C_{OVD}, C_{OVS} and C_{OVGB} can be approximated as

$$C_{OVD} = W_{eff} C_{GD0} \tag{4.34}$$

$$C_{OVS} = W_{eff} C_{GS0} \tag{4.35}$$

$$C_{OVGB} = L_{eff} C_{GS0} \tag{4.36}$$

where W_{eff} is the effective channel width, L_{eff} is the effective channel length andC_{GS0}, C_{GD0} and C_{OVGB} are the zero bias gate/source and gate/drain and gate/bulk capacitance per unit length respectively.

The gate capacitances C_{GS}, C_{GD}, and C_{GB} depend on the operating region. The equations that describe each of these capacitances are summarized in Table 4.3.

Table 4.3. *Channel capacitance of MOS device for different operation region*

Operation region	C_{GB}	C_{GS}	C_{GD}
Cutoff	$C_{ox}W_{eff}L_{eff}$	0	0
Linear	0	(1/2) $C_{ox}W_{eff}L_{eff}$	(1/2) $C_{ox}W_{eff}L_{eff}$
Saturation	0	(2/3) $C_{ox}W_{eff}L_{eff}$	0

where C_{ox} is the gate oxide capacitance per unit area, and is defined as:

$$C_{ox} = \frac{\varepsilon_{ox}\varepsilon_0}{T_{ox}} \tag{4.37}$$

where, ε_{ox}, is the dielectric constant, ε_0, is the permittivity of free space and T_{ox}, is the dielectric thickness. Based on the above consideration the effective gate capacitance may be approximated as:

$$C_G = C_{ox}W_{eff}L_{eff} + C_{OVD} + C_{OVS} + 2C_{OVGB} \tag{4.38}$$

Inverter capacitances.

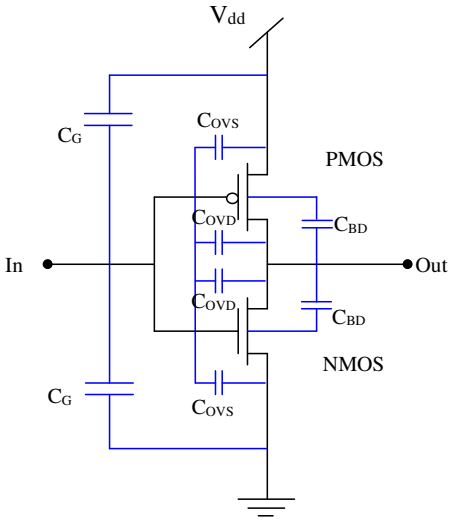


Fig.4.21. Parasitics capacitances influencing the transient behavior of CMOS inverter.

The inverter capacitances are shown in Fig.4.21. The total input inverter capacitance is determined by the width of NMOS and PMOS transistors. Assuming that the PMOS transistor is two times wider then NMOS, the total input capacitance for minimum size inverter is given as:

$$C_{IN}^{inv} = C_G^{nmos} + C_G^{pmos} = (1+2)C_G \quad (4.39)$$

Since in standard CMOS inverter one NMOS and one PMOS drain are connected to the gate output node, the parasitic output capacitance is described:

$$C_{OUT}^{inv} = C_{BD}^{nmos} + C_{BD}^{pmos} = (1+2)C_{BD} \quad (4.40)$$

Based on the BSIM3v3 and BSIM4 parameters and on the formulas described above ICAL calculates the input capacitance and output resistance of a given repeater. This parasitic buffer components will be further required in the ICAL optimization unit in order to determine the optimal number and size of buffer needed in the system.

4.5 OPTIMIZATION UNIT

This section is focuses on describing the optimization methods incorporated into ICAL program, which are commonly used for determining optimal CDN design. The most important method used to optimize the VLSI interconnect systems, especially the clock distribution network is the buffer insertion method. Since the number of repeaters used in clock system is optimized in terms of signal propagation time, it is necessary to accurately calculate the delay introduced by interconnects. This subchapter will present two RC and RLC analytical formulas used in the calculation of propagation time, and the buffer insertion methods associated with these formulas. All described formulas and repeater insertion methods are incorporated into ICAL program. Depend on the considered clock system parameters (i.e. technology, operating frequency etc.) the user can choose appropriate optimization methods.

4.5.1 RC delay calculations.

There are several papers and texts that discuss the modeling of propagation delay for a CMOS gate driving a capacitive load [ELM-48], [SAK-93], [DEN-90]. Current methods base on the SPICE simulation or analytical formulas. In this section the analytical solution will be described. There are two definition of interconnect delay time. The first one is the delay from 50% point of the input waveform to 50% point of the output waveform, while the second one correspond to 90% point of the waveform [BAK-90]. Traditionally the delay required to reach 50% of the logic swing is referred as *delay time*.

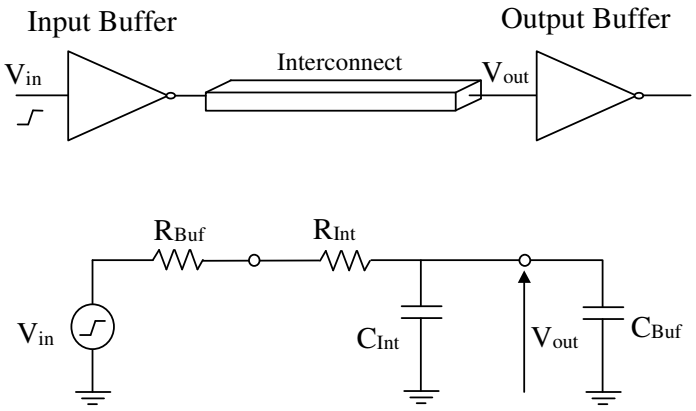


Fig.4.22. Interconnection delay model. The signal delay is modeled using the circuit shown above. The total path delay includes the effects of the driver resistance, device load capacitance, and the distributed RC interconnect load.

A simple equivalent circuit that is usually used in delay calculation is shown in Fig.4.22, where R_{Buf} is the buffer output resistance, C_{Buf} is the input capacitance of the driven gate, and R_{Int} ,C_{Int} are the interconnect resistance and capacitance respectively. For this simple RC circuit the output response for a unit step input ($V_{in}(t)$ =0 for $t < 0$ and $V_{in}(t)$ =1 for $t \geq 0$) is given as:

$$V_{out}(t) = 1 - \exp(\frac{-t}{\tau_{RC}}) \qquad (4.41)$$

where τ_{RC} is the time constant of the circuit shown in Fig.1. and is given by:

$$\tau_{RC} = (R_{Buf} + R_{Int})(C_{Buf} + C_{Int}) \tag{4.42}$$

The most widely used delay formula is the expression given by Elmore [ELM-48]. His delay formula is defined to be the first moment of the system impulse response. Despite not being highly accurate, the Elmore delay is widely used by industry for fast delay estimation. The Elmore delay formula for 63.2% signal threshold is given as :

$$T_{Elmore}^{63.2\%} = 0.5R_{Int}C_{Int} + R_{Buf}C_{Int} + R_{Int}C_{Buf} + R_{Buf}C_{Buf} + R_{Int}C_{Int} \tag{4.43}$$

Sakurai [SAK-93] also derived response calculation for distributed RC lines. He calculates the time-domain response from the transfer function using the Heaviside expression over poles of the transfer function. He then approximated the response using a single pole and observed the variation of delay with respect to source and load parameters. His closed-form expression is given as:

$$T_{\upsilon} = 0.1R_{Int}C_{Int} + \ln\left(\frac{1}{1-\upsilon}\right)(R_{Buf}C_{Int} + R_{Int}C_{Buf} + R_{Buf}C_{Buf} + 0.4\,R_{Int}C_{Int}) \tag{4.44}$$

where T_{υ} is the delay from $t = 0$ to the time when the normalized voltage at the end point reaches υ ($=V/V_{dd}$). Note that Sakurai's heuristic delay formula is almost identical to the Elmore delay equation.

4.5.2 RC repeater insertion method.

Using the repeaters that divide the interconnection into smaller subsections is one approach to reduce the interconnect delay. However, insertion of a non-optimal number of repeaters can increase overall propagation time. A significant amount of work has been

done to determine an optimal solution for the number and size of a repeaters used in interconnect [BAK-85], [HED-87], [GIM-90], [WU-90], [ALP-97], [ADL-00], [AJA-01] . By the far, the most popular approach to boost interconnect performance is the optimal insertion method proposed by Bakoglu [BAK-85]. The interconnect resistance and capacitance depend linearly on wire length. As the line gets longer, the propagation time increase proportionally to the square of the interconnection length. The first order expression of interconnect delay time for line from Fig.4.23.a) is given as:

$$T_{DELAY} = RCl^2 \tag{4.45}$$

where l is wire length, R and C are the interconnect resistance and capacitance per unit length respectively. In order to minimise the delay time, a global interconnect is divided in subsections, each with its own buffer (Fig.4.23.b)). The insertion of buffers (or repeaters) reduces the dependence of interconnect length on delay from quadratic to linear. Since, the additional inserted repeaters increase the overall gate delay, there is an optimal number of buffers that should be inserted into RC line to minimise the overall propagation delay.

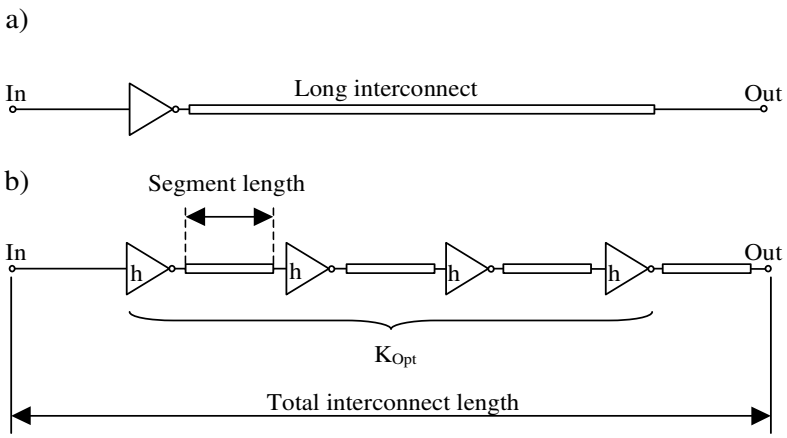


Fig.4.23. Typical on-chip interconnect system. a) Interconnect with single driver. b) Interconnect with K repeaters, each repeaters is h time that a minimum-size.

The signal delay for line from Fig.4.23.b) can be calculated using the simple delay expression like (4.46), where, K is number of repeaters, T_{Buf} is buffer internal delay.

$$T_{DELAY} = \frac{RCl^2}{K} + (K - 1)T_{Buf} \quad (4.46)$$

Using (4.46), the optimal number of buffers can be found. However, it is necessary to take into account some additional effects. For example the buffer delay, T_{Buf}, depends on the interconnect load and the driver size. To optimize both the number and size of the buffers, Sakurai delay formula can be modified as:

$$T_{DELAY} = \frac{0.377R_{Int}C_{Int}}{K} + 0.693(R_{Buf}C_{Int} + R_{Int}C_{Buf} + KR_{Buf}C_{Buf}) \quad (4.47)$$

where R_{int} and C_{Int} are the interconnect resistance and capacitance respectively. Since the repeater current-drive capability is directly proportional to its W/L ratio, the propagation time can be improved by increasing the size of the buffers. Increasing the buffer size reduces transistor resistance but increases the capacitance by the same factor. Setting h to be the buffer size gives

$$R_{Buf} = \frac{R_o}{h} \quad (4.48)$$

$$C_{Buf} = hC_o \quad (4.49)$$

where R_o and C_o are the minimal buffer output resistance and input capacitance respectively. And substituting into (4.47), we get:

$$T_{DELAY} = \frac{0.377R_{Int}C_{Int}}{K} + 0.693\left(\frac{R_oC_{Int}}{h} + R_{Int}C_oh + KR_{Buf}C_{Buf}\right) \quad (4.50)$$

By setting $\delta T_{DELAY}/\delta K$ and $\delta T_{DELAY}/\delta h$ to zero the optimal number of buffers and the optimal buffer size are given as.

$$K_{Opt} = \sqrt{\frac{0.377 R_{Int} C_{Int}}{0.693 R_o C_o}} \tag{4.51}$$

$$h_{Opt} = \sqrt{\frac{R_o C_{Int}}{R_{Int} C_o}} \tag{4.52}$$

Bakoglu summarises that, in order to drive the interconnect line optimally, the delay of the repeaters should be equal to the delay of interconnect. Thus, the optimum number of buffers K_{Opt} depend on the ratio of the interconnect delay $R_{Int}C_{Int}$ to the gate delay R_oC_o. The size of the repeater is independent on the length of the interconnect since the C_{Int}/R_{Int} ratio is the same for all wire lengths in a particular metal layer. The optimum repeater size h_{Opt} is chosen such that the output buffer resistance is close to the interconnect resistance of each section. By using the repeaters an interconnect may be made narrower and still operate with the same propagation delay. This leads to reduction in wire area, however increase the area of active device.

4.5.3 RLC delay calculations

Although the formulas described in the subchapter 4.5.1 have been widely used for interconnect timing analysis, they cannot accurately estimate the delay for *RLC* interconnect lines, which are the appropriate representation for interconnects whose inductive impedance cannot be neglected. The presence of interconnect inductance L_{Int} introduces ringing and overshoot phenomena not found in RC circuits. In 1995 Krauter [KRA-95] proposed to improve Elmore delay model by using higher order moments. Next Kahn and Muddu [KAH-97] developed a first analytical model for RLC interconnect using the first and second moments to characterize the response of RLC line. However, the solution developed by Kahn and Muddu are composed three different formulas for the case of real, complex and multiple pole.

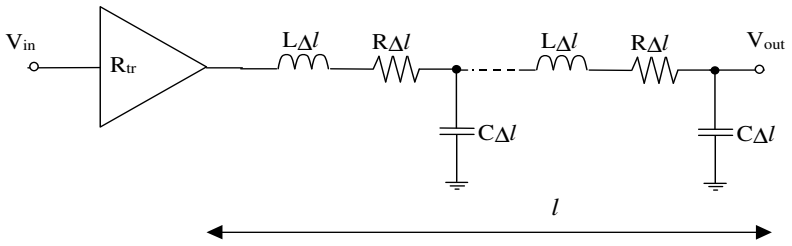


Fig.4.24. Equivalent circuit of a gate driven single distributed RLC line.

The first analytical closed-form formula is presented by Ismail and Friedman [ISM-00]. This delay model considers all damping conditions of an RLC circuit including the underdamped response, which was not considered by the Elmore delay approach. For the gate driving an distributed RLC line presented in Fig.4.24. the 50% propagation delay is given as:

$$T_{RLC}^{50\%} = [\exp(-2.9\zeta^{1.35}) + 1.48\zeta]\omega_n \tag{4.53}$$

where ω_n is given by:

$$\omega_n = \frac{1}{\sqrt{L_{Int}(C_{Int}+C_{Load})}} \tag{4.54}$$

ζ is called damping factor and is given as:

$$\zeta = \frac{R_{Int}}{2}\sqrt{\frac{C_{Int}}{L_{Int}}}\,\frac{R_{tr} + C_{Load} + R_{tr}C_{Load} + 0.5}{\sqrt{1+C_{Load}}} \tag{4.55}$$

For the small damping factor, ζ, the inductance effect increase and the response is underdamped, for large ζ the inductive effect is low and the signal response is overdamped. For large ζ (small inductive effects) delay equation given by Ismail and Friedman becomes as follows:

$$T_{RLC}^{50\%}(\zeta \to \infty) = 0.37R_{Int}C_{Int} + 0.74(R_{Buf}C_{Int} + R_{Int}C_{Load} + R_{Int}C_{Int} + R_{Buf}C_{Load}) \quad (4.56)$$

Note the similarity of this expression to (4.43) and (4.44), which describe the propagation of RC interconnect. Thus, the delay expression for an RLC tree has the same accuracy characteristic as the classical Elmore and Sakurai expressions.

4.5.4 RLC repeater insertion method.

Ismail and Friedman studies in [ISM-98], [ISM-99b], [ISM-00], [ISM-01] the problem of repeater insertion method in RLC interconnect. Traditionally, repeaters are inserted into RC line to partition an interconnect line into shorter section. Ismail an Friedman applied the same idea to RLC interconnect. They showed that in RLC line, the repeater area for minimum delay time is between the maximum repeater area in the RC case and the zero repeater area in the LC case. Since, the repeater area tends to decrease as inductance effects increase, inserting repeaters based on RC model and neglecting inductance results in larger repeater area than necessary. The closed form expression for optimal number and size of repeaters that need to be inserted along the RLC interconnect to achieve the minimum propagation delay is given as:

$$K_{Opt}^{RLC} = \sqrt{\frac{R_{Int}C_{Int}}{2R_oC_o}} \frac{1}{[1 + 0.18(T_{L/R})^3]^{0.3}} \quad (4.57)$$

$$S_{Opt}^{RLC} = \sqrt{\frac{R_oC_{Int}}{R_{Int}C_o}} \frac{1}{[1 + 0.16(T_{L/R})^3]^{0.24}} \quad (4.58)$$

where

$$T_{L/R} = \sqrt{\frac{L_{Int}/R_{Int}}{R_oC_o}} \quad (4.59)$$

Note that the optimal number and size of repeaters in (4.57) and (4.58) are the same as the expression given by Bakaglu [BAK-85] for the special case of an RC line where $L_{Int} \rightarrow 0$ (or $T_{L/R} \rightarrow 0$). Both the number and the size of repeaters decrease as inductance effect increases.

4.5.5 Cascaded buffers.

Another method implemented in ICAL program used to optimize the interconnect system in terms of propagation time is insertion of the cascaded buffers. This method is especially useful in order to drive a large capacitive loads at high speeds. The cascaded buffers consist of a number of CMOS inverters with gradually increasing driving capability according to Fig.4.25. [NEM-84], [HED-87], [LI-90]. This structure consists of a series of inverters where each successive inverter is *f* time larger then the previous one. So the input capacitance is as small as possible and the last inverter is large enough to drive the large capacitive load. The total delay through the cascade is the sum of the delay through each of the inverters. Cascaded drivers are useful when the parasitic interconnect resistance is small compared to buffer output resistance. The analytical Elmore expression for the propagation delay in tapered buffer may now be written as:

$$T_{DELAY} = 0.377 R_{Int} C_{Int} + 0.693\left(\frac{R_o}{f^{N-1}} C_{Int} + (N-1) f R_o C_o + R_{Int} C_o\right) \qquad (4.60)$$

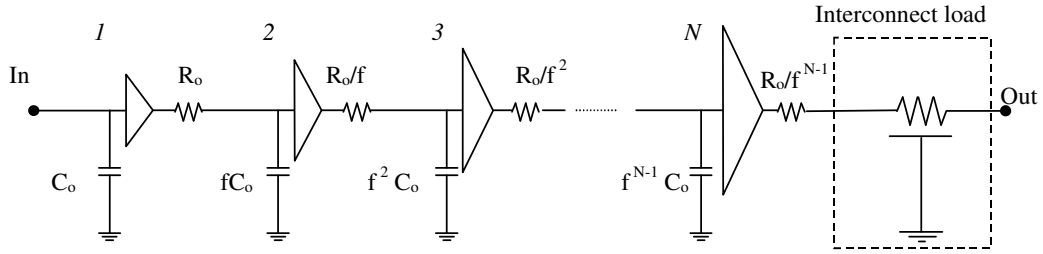


Fig.4.25. The cascaded driver consists of a series of inverters. (where R_o and C_o are the output resistance and input capacitance of minimum-size inverter)

It can be showed that the minimum delay is achieved when the ratio between the transistor channel width in adjacent stages is exponentially tapered. Optimal number of stages *N* and optimal tapered factor *f* are defined by (4.61) and (4.62) respectively [JAE-75].

$$F = \frac{W_i}{W_{i-1}} = e \approx 2.72 \tag{4.61}$$

$$N = \ln\left(\frac{C_{Int}}{C_o}\right) \tag{4.62}$$

where W_i is the width of the device in the *i*th stage of tapered buffer, *e* is the base of the natural logarithm. However, it is the classical ratio for performance, but it is not a good choice for low-power design. Since the total time delay increases slowly with larger *f* , tapered factor fixed in ICAL is greater then *e,* which save power dissipation with little increase in propagation time.

4.6 CONCLUSION.

In this chapter the tool called ICAL has been presented. This program provides designers with the capability to model, evaluate, predict and optimize global clock distribution networks for future technologies. The models and the assumptions used by ICAL are precisely described. For example the formulas to accurately estimate the interconnect resistance, capacitance and inductance as well as the device parameters are presented. These formulas are used by the ICAL optimization unit to estimate the optimal number and size of the needed repeaters. This can be done based on the RC or RLC buffer insertion methods. Once the optimal buffer size and optimal segment length are determined, based on the regularity of H-tree structure ICAL creates the SPICE netlist where the interconnects are replaced by RC or RLC distributed lines coupled by buffers designed as CMOS inverters. The power dissipated in the system can be extracted from transistor-level simulations or from the implemented analytical formulas.

V. Optical Interconnects

Chapter V

Optical Interconnects

5.1 INTRODUCTION.

The optical interconnections are recognized as a very attractive solution that should allow solving the majority of on-chip global electrical interconnect problems. Their advantages such as large information capacity, no electromagnetic wave interference, high interconnection density, low power consumption, high speed, and planar signal crossing made that their application to IC chips has been the subject of many research at last years [WU-87], [FAN-95], [LEV-00], [LEE-00], [CRI-01], [HIM-01]. It requires, however, the integration of optical and electronic devices on the same chip what generate now technological problems. Such problems do not occure or are much smaller in the case of optoelectronic device integration on module or board levels and many such system have been already designed and justified in term of cost, performance, and compatibility with existing system software and hardware.

At the most basic level, one can say that the physics of optical and electrical signal propagation is very similar. The physical similarities and differences between optical and electrical interconnects have been presented by Miller [MIL-96]. In both optical and electrical case, the signals are carry by electromagnetic waves. In the low-loss coaxial cable the signals move essentially at the velocity of light, which is similar to optical interconnect. In fact, signals typically travels slower in optical fibers and in on-chip interconnect because of dielectric constant in fiber and parasitic resistance in electrical wire, respectively. The fundamental differences between optical and electrical signal propagation are shown in Fig.5.1. The optical case is characterized by shorter wavelength, the higher frequency, and the larger energy of signal carriers i.e. photons.

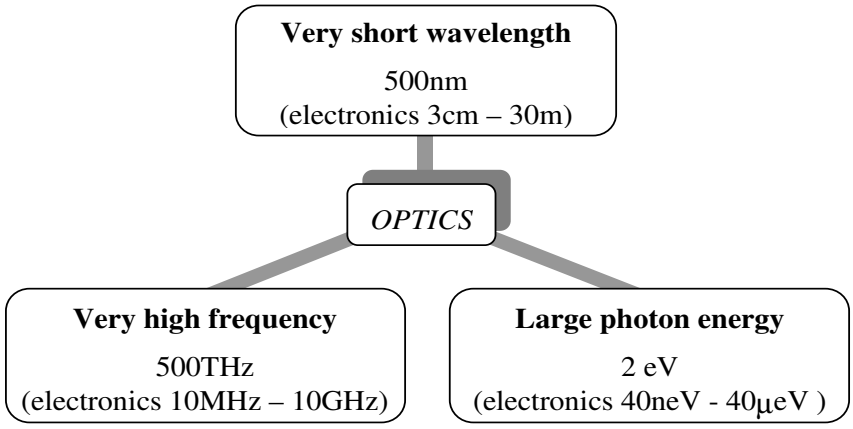


Fig.5.1. Fundamental physical differences between optics and electronics.

Most of the potential advantages of optical solution arise from these fundamental differences. For example, in the optical interconnection, in contrast with electrical one, no frequency-dependent loss or frequency-dependent crosstalk occurs. An optical system might potentially work up to 500 GHz because the frequency of modulation has essentially no effect on the propagation of the light signals. Additionally, the optical interconnect provides perfect voltage isolation between two connected electronic circuits, and this way allows solving the matching problem in electronic system. In order to have benefits from the advantages of optical signal propagation, it is necessary to implement optical interconnect into conventional silicon integrated circuits. A technology that allows easy conversion between electronics and optics and vice versa is crucial for future development of optoelectronic VLSI (OE-VLSI).

An optical interconnection has at least three parts distinguished in Fig.5.2. the transmitter that is a source of optical signal, the receiver that is a detector of optical signal , and the optical channel that creates a path between them. On the transmit side, an information source produces the data stream that is encoded and sent to the appropriate drive circuit used to modulate the optical signal generated by a light emitting diode (LED) or a semiconductor laser.

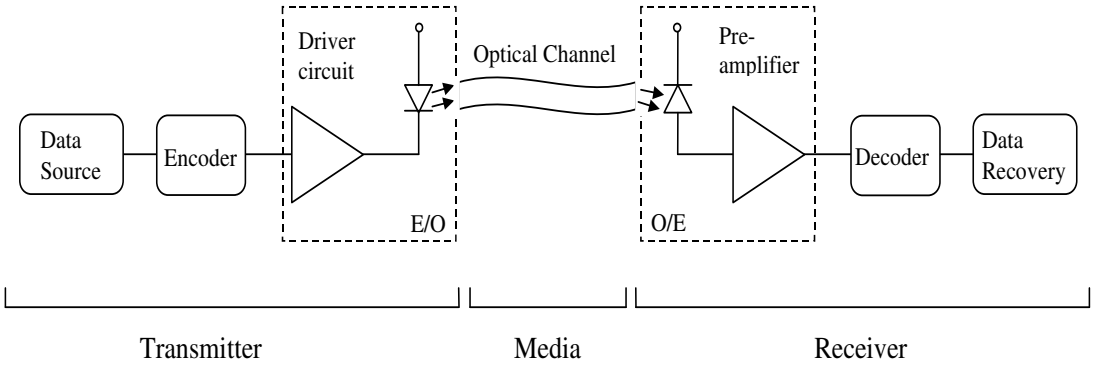


Fig.5.2. Block diagram of typical optical link.

The signal propagates through free space or through a waveguide such as an optical fiber until it reaches the photodetector on the receiver side. The photodetector converts the optical signal into an electric one that is sensed by the preamplifier and regenerated to a sufficiently large voltage signal from which the original data can be recovered in a demodulator. Although this optical interconnection architecture has been already applied with success in many practical cases like e.g. optical telecommunication lines, the technology allowing its implementation as optical interconnection in conventional VLSI is not yet mature. The research progress in this area has been, however, substantial in recent years. This chapter has reviews the optical technology available for implementing the optical communication system

5.2 OPTICAL RECEIVER.

5.2.1 General structure of conventional receiver.

The optical receiver circuit is one of the most critical components of the optical link. Its role is to convert back the optical signal that can be attenuated by noise and dispersion into electrical one and to recover the data transmitted through the optical link.

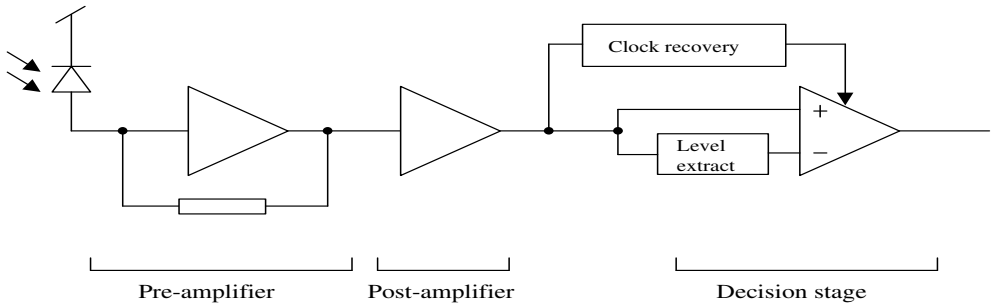


Fig.5.3. Block diagram of conventional telecommunications receiver.

The receiver design can be generally break down into the blocks shown in Fig.5.3. The incoming optical signal is converted into an electrical one at the photodetector. The pre-amplifier converts the input photocurrent into a low-level voltage. Its main objective is to minimize the electronic noise added to the optical signal. Due to amplification and bandwidth requirements, usually a post-amplifier is the next stage in the design. It amplifies small voltage signals into rail-to-rail voltage. The decision circuit produces a regenerated logic signal that is often re-timed with a clock extracted from the data stream. All receiver components shown in Fig.5.3., with exception of the photodiode, are standard electrical components, and can be easily integrated with other circuits on the IC chip using standard silicon technology.

5.2.2 Photodiodes.

The photodetectors can be manufactured as photodiodes or phototransistors. For high-speed optical communications, however, the photodiodes are preferred due to their superior frequency response. The most important performance criteria that must follow at selecting a photodetector for the optical receiver are its wavelength, speed and responsivity.

The wavelength of photodiode depends on the materials it is manufactured from. In the case of photodiodes adopted for most of long distance optical communications systems, it is fixed at 1.3μm and 1.55μm what corresponds to the transmission windows of silica

fibers. Therefore the photodiodes designed for this application are manufactured from compound semiconductor materials $A_{III}B_V$ type like GaAs, InGaAs or InGaAsP. The photodiode speed depends on its parasitic capacitance that is determined by the photodiode size and structure. Photodiode responsivity, $\Re$, quantifies the photoelectric gain of a photodetector and is defined by:

$$\Re = \frac{\eta q}{hv} \approx \frac{\eta \lambda}{1.24} \tag{5.1}$$

where, η - the detector quantum efficiency, q - electron charge constant, h - Planck constant, v - optical frequency and λ - wavelength. It is the ratio of the photocurrent (in short-current conditions) generated for each watt of incident light power. Typical photodetector responsivity varies from 0.4 to 1.2 depending on the material and fabrication method.

A reverse-biased *p-n* junction is the simplest photodiode structure. When such a *p-n* junction is illuminated with light, electrons in the valence band can absorb the energy of incident photons if the photon energy hv is at least equal to the bandgap energy W_g. This way the energy of valence electrons becomes sufficiently large to move them to the conduction band, what corresponds to the creation of an electron-hole pair, i.e. two new free carriers. If it occurs in the p-n junction depleted region, the carriers will quickly separate leading to a current flow through the junction and the resulting current will be proportional to the incident optical power.

Due to its low responsivity, ordinary *p-n* diodes are insufficient detectors for fiber optic systems. A simply suitable modification that can improve its performances is the introduction of the third almost intrinsic low doped layer between the *n* and *p* layers creating the *p-n* junction. It is well known *p-i-n* structure that is shown in Fig.5.4. in a form of PIN photodiode, probably the most widely used photodetector solution. Its advantage consists in the fact that even at low reverse voltage, the depleted region fill in the whole *i*-layer, the area when the carrier separation can take place is very large and as result, the responsivity of the diode can be large too

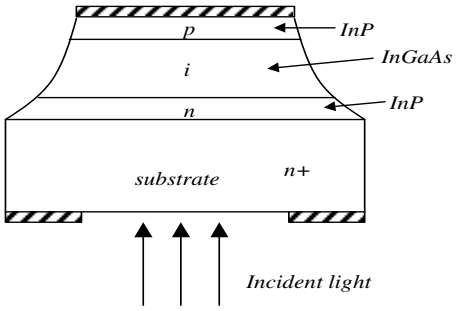


Fig.5.4. InGaAs PIN photodiode structure.

One limitation of the PIN photodiode is the lack of internal gain what means that any incoming photon can produces one electron-hole pair only. This drawback can be corrected if the PIN diode is designed as the Avalanche Photo Diode (APD) in which the avalanche generation of electron-hole pairs is employed to photocurrent enlargement. In such a photodiode, carriers generated by light create other carriers via impact ionization, providing an internal gain. Unfortunately, APD photodiodes require high-voltage power supplies for their operation. The voltage can range from 30 or 70 Volts for InGaAs APDs to over 300 Volts for Si APDs what leads to undesired circuit complexity. The APDs are also very temperature sensitive what introduces additional requirements concerning the circuit complexity. As result, they are not so attractive in practical applications as PIN photodiodes that remains the best choice for most high-speed systems

5.2.3 Preamplifiers

The preamplifier plays a crucial role in determining many aspects of the overall performance of the receiver including speed, sensitivity, and dynamic range. Usually, the role of preamplifier is to converts the input photocurrent to a low-level voltage for further processing. The proper design of preamplifier requires an appropriate trade-off between bandwidth and sensitivity. Generally three solutions of preamplifier representing by two topologies depicted in Fig.5.5. and Fig.5.6. are commonly used. They are: low- or high-impedance front-end topology presented in Fig.5.5. and transimpedance amplifier presented in Fig.5.6.

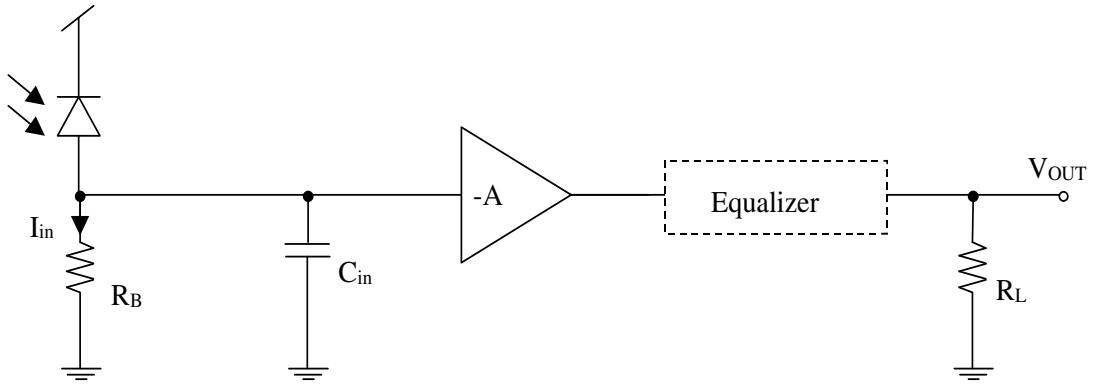


Fig.5.5. Schematic diagram of open-loop preamplifier configuration.

The low-impedance front-end design [BAR-94] is characterized by a low value of the bias resistor R_B, (usually 50Ω) and an open-loop amplifier configuration. The photodiode current signal I_{in}, is converted into a voltage on the bias resistor R_B, and the resulting voltage signal is buffered by the voltage amplifier. The capacitance C_{in} represents, in the scheme in Fig.5.5, the total capacitance associated with the photodiode and the amplifier. The low-impedance front-end has a very broad bandwidth and good dynamic range. Low resistance value affects, however, the sensitivity of the amplifier due to the small input voltage, load resistance and high thermal noise generated in the bias resistor R_B.

The high-impedance front-end design [SMI-82], [MUI-84], [ALE-97] is characterized by a large value of the bias resistor R_B. It reduces the thermal noise and improves the receiver sensitivity. However, the frequency bandwidth is limited by the RC time constant at the input. In order to increase the receiver bandwidth to the desired range, sometime, an equalizer is placed after the amplifier (droped box in Fig.5.5.). The equalizer acts as the filter that attenuates low-frequency components of the signal and restores a flat transfer function to the system. This leads, however, to increase the complexity of the circuit.

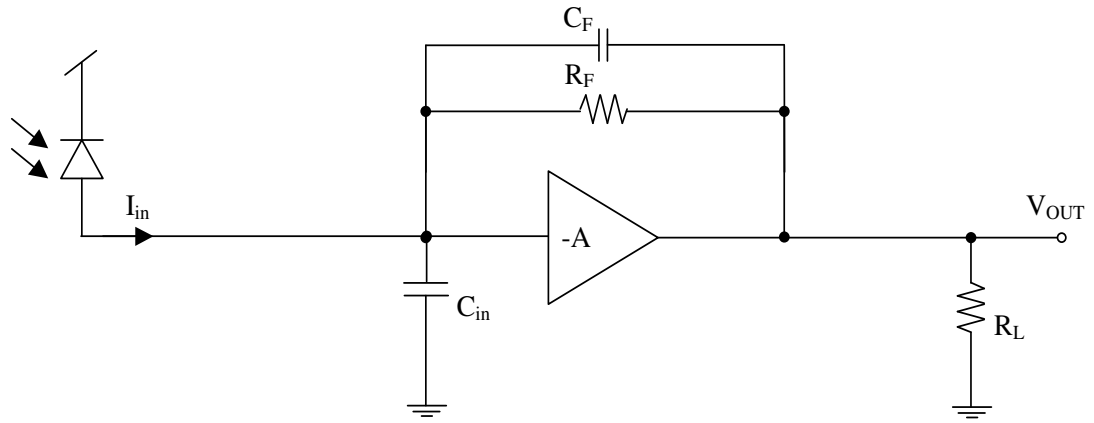


Fig.5.6. Schematic diagram of transimpedance preamplifier configuration.

The transimpedance amplifier design (TIA) [NAK-99], [OHA-99] is currently the most widely used preamplifier structure for high-speed optical receivers. This configuration provides a compromise between low- and high-impedance configurations. Its merit is to combine a relatively high transimpedance gain with high speed. The basic diagram of the transimpedance amplifier with negative feedback is shown in Fig.5.6. The feedback resistor, R_F, placed across the gain stage, determines the transimpedance, and thus the sensitivity of the amplifier. Now, the resistor can be large because the negative feedback reduces the effective resistance seen by the photodiode by a factor of (1 + A), where A is the open-loop voltage gain of the amplifier. Large feedback resistor increases the sensitivity of the amplifier, but simultaneously reduces the amplifier speed.

Among these configurations, the transimpedance amplifier is selected over the others and used in the next analysis. This selection was based on the relatively wide bandwidth and good noise level of this structure.

In order to determine the minimum acceptable input signal and the accuracy of the signal transmission in optical system it is necessary to perform the noise consideration of the optical receiver. The standard theory of photoreceiver noise was developed by Personick [PER-73], [SMI-82]. While the formulation given by Personick is mathematically correct, it introduces several assumptions, which generally do not hold true in practice. Based on this work Morikuni [MOR-94] considered the effect of incorporating a realistic transfer function into the conventional photoreceiver analysis.

The transimpedance transfer function of the preamplifier circuit presented in Fig.5.6. can be expressed as:

$$Z_T(\omega) = \frac{V_{out}(\omega)}{i_{in}(\omega)} = \frac{R_F\left(\frac{A'_\upsilon}{1 + A'_\upsilon}\right)}{1 + j\omega R_F\left(C_F \frac{C_{in}}{1 + A'_\upsilon}\right)} = \frac{A + j\omega B}{C + j\omega D + (j\omega)^2 E} \tag{5.2}$$

where A_υ is the open-loop voltage gain modified to take into account the effect of feedback loading and the constant A-E are [MOR-92]:

$$A = R_o(1 - g_m R_F) \tag{5.3}$$

$$B = R_o R_F C_F \tag{5.4}$$

$$C = 1 + g_m R_F \tag{5.5}$$

$$D = R_o(C_{in} + C_{out}) + R_F(C_{in} + C_F) + g_m R_F R_o C_F \tag{5.6}$$

$$E = R_F R_o[(C_{in} + C_{out})C_F + C_{in}C_{out}] \tag{5.7}$$

where R_o is the output resistance, g_m is the transconductance, C_F is the parasitic feedback capacitance, C_{in} is the sum of photodiode and amplifier input capacitances, and C_{out} is the sum of the load, next stage and amplifier output capacitances as is present in the small-signal representation of the transimpedance amplifier shown in Fig.5.7.

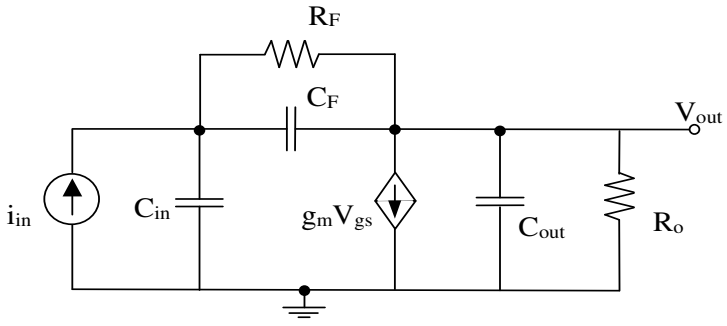


Fig.5.7. Small-signal representation of transimpedance amplifier.

The equivalent input noise current introduced by the photodiode and transimpedance amplifier described by the transfer function of (5.2) is expressed as:

$$\sqrt{i_N^2} = [\, 2q(I_{gate}+I_{dark})+ \frac{4kT}{R_f} \,] \frac{C}{4D} + 4kT\Gamma \frac{C^2}{16\pi^2 DE} \frac{(2\pi C_{in})^2}{g_m} \qquad (5.8)$$

where I_{gate}, I_{dark} are the transistor gate and photodiode dark current respectively, k is Boltzmann's constant, C_T is the input capacitance, g_m is the transconductance, Γ is the excess channel-noise factor, T is temperature and C,D,E are transimpedance constants described above. The first term of (5.8) is the shot noise contribution due to transistor gate current and the detector dark current, the second term is the thermal, or Johnson noise contribution due to feedback resistor, and the third term is the contribution due to thermal noise in the conducting channel of the amplifier drive transistor. This expression is general, and can be used for any amplifier configuration that transfer function can be expressed in terms of physical circuit. However, if absolutely nothing is known about the receiver circuit, it may be necessary to use less accurate signal-dependent, circuit independent noise expression given by Personick.

$$\sqrt{i_N^2} = [2q(I_{gate}+I_{dark})+ \frac{4kT}{R_f}]I_2 B + 4kT\Gamma \frac{(2\pi C_{in})^2}{g_m} I_3 B^3 \qquad (5.9)$$

where B is the bit rate and I_2, I_3 are the weighting functions, which for rectangular pulse shape are equal 0.55 and 0.086 respectively, for Gaussian pulse shape, both I_2 and I_3 are bigger than 1.

5.3 OPTICAL SOURCE.

5.3.1 Semiconductor lasers.

The role of optical source is to convert an electrical input signal into the corresponding optical signal and then launch it into the optical fiber serving as the transmission medium. The two primary light sources used in telecommunications are light emitting diodes (LED's) and semiconductor lasers.

In a simplest form, LED is a forward-biased p-n junction, which emits light through spontaneous emission. Light emission takes place when the electrons in the conduction band recombine with holes in the valence band. The photons are emitted in a random direction with no phase relationship among them. Therefore, the drawbacks of the LED are low output power, higher divergence degree, and wide optical spectral bandwidth which are not suitable for high-speed communication. However, the LED are simply for fabrication, high reliability and are less expensive then semiconductor lasers.

Laser emits light through the process of stimulated emission rather then spontaneous emission. Laser is an acronym for light amplification by the stimulated emission of radiation. In contrast to the spontaneous emission, the stimulated emission is initiated by an existing photons. The remarkable feature of this process is that one incident photon after stimulated emission becomes two photons with the same frequency, direction and phase. If the stimulated emission can dominate over absorption processes, the coherent light can be emitted. In order for stimulated emission to have a visible effect, a population inversion on upper level must be created. There are two broad kinds of lasers, edge emitting lasers and vertical cavity surface emitting lasers (VCSELs) presented in Fig.5.8.a) and Fig.5.8.b) respectively.

In the edge emitter, which has traditionally dominates the semiconductor laser market, photons are emitted out of one edge of the semiconductor wafer after rebounding off mirrors that have been literally cleaved out of the crystalline substrate.

In the VCSEL [GEO-92], [SAL-95] laser photons bounce between mirrors grown into the structure and then emit vertically from the wafer surface. VCSELs that can be grown by the thousands on a single wafer, have significant advantages over the edge-emitting lasers in the areas of lower manufacturing, packaging, alignment, and testing

costs, as well as lower power losses and higher reliability. As is the case for all laser diodes, VCSEL have a threshold current below which there is no coherent light emission. Above the threshold the device can work very efficiently and can produce a diffraction-limited light beam with a very low numerical aperture. VCSEL's are a promising devices for low-power optical interconnections [KOS-93], [FIE-95], [ZHO-97], [MIC-97], [KAZ-98], [DRG-99] and optical informations processing [SHI-96] as they possess both efficient vertical emission, an essential ability of integration [HAS-91], [SJO-98], [LOU-99] and the ability to operate either as source or receiver [KOS-91], [ROS-96], [LIM-97]. VCSEL can be classified according to the technique used to define the extend of the laser cavity, the most popular are ion-implantation and selective oxidation. The fabrication of VCSEL is reviewed in [CHO-97].

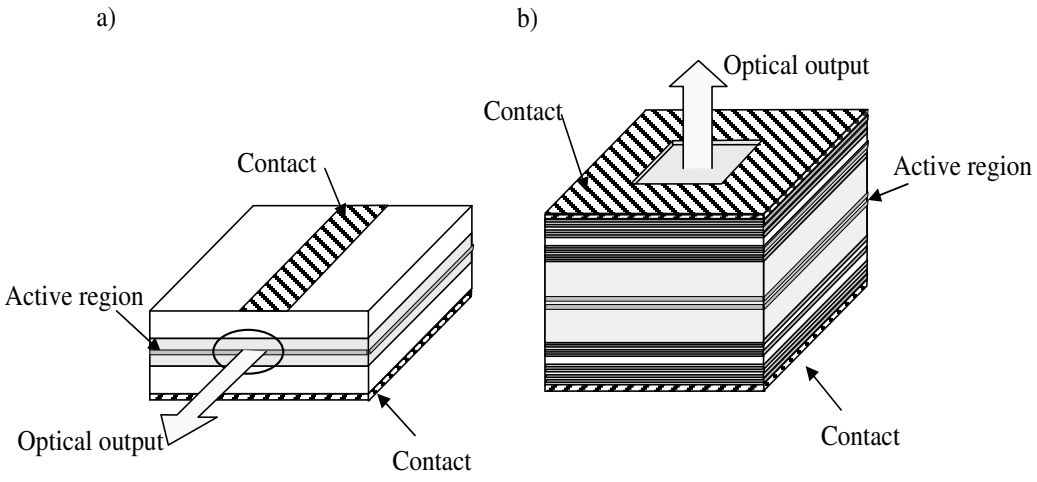


Fig.5.8. Schematic geometry of semiconductor lasers. a) Edge emitting laser. b) Vertical cavity surface emitting laser.

VCSELs are a strong candidate as a transmitter device as they have improved significantly in the last few years. The reduction of threshold currents has solved the problem of excess power dissipation, making VCSEL-based interconnects very promising. Recently, optical interconnects with VCSELs arrays have been demonstrated [FIE-95], [MIC-97]. As a light emitter, VCSEL require a minimum voltage drive approximately equal to or larger than the material bandgap. With technology scaling, it is predicted that

operating voltages will be less than 0.8 Volts by 2011 [ITRS], this eliminate the necessity of additional high-voltage lines. By placing the emitter off-chip, thermal effects can be also managed with less difficulty.

5.3.2 Laser driver circuits.

The role of laser driving circuits is to provide electrical power to laser and to modulate the light output in accordance with the signal that is to be transmitted. Since, semiconductor laser are biased near threshold and then modulated through electrical time-depended signal, the driving circuit must supply a constant bias current (dc) and also modulate the electric signal.

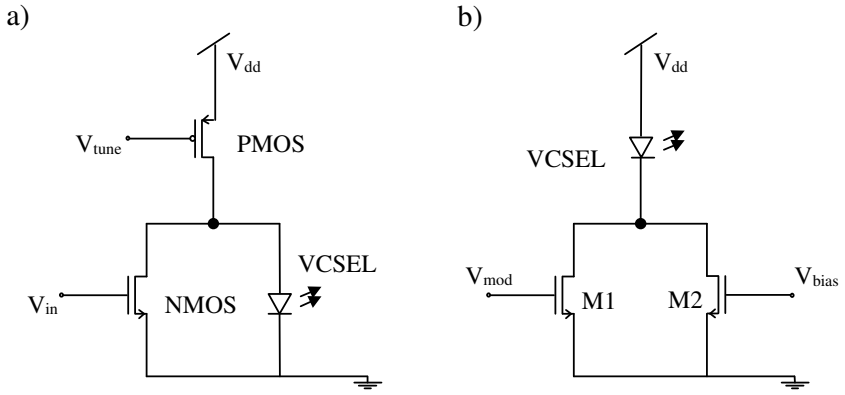


Fig.5.9. Laser driver circuits.

The simple two-transistor VCSEL driver circuits proposed by [KRI-99] is shown in Fig.5.9.a). This CMOS circuit is based on a current-shunting principle which provides a low-area, tunable-power circuit. The PMOS transistor is used to supply an adjustable current through the laser, and the NMOS transistor is used to quickly shunt the current into and out of the VCSEL for digital operation. Another CMOS VCSEL driver circuits has been introduced in [MAT-97]. This circuit shown in Fig.5.9.b) consists of two NMOS transistors. Transistor M2 is designed to bias the VCSEL above threshold while the other

M1 is used to provide the modulation. Here the current flowing continuously is lower then in the shunt driver described previously.

5.4 PASSIVE OPTICAL COMPONENTS.

Waveguides are constructed by a system of material boundaries that allow control of wave propagation within a specified region. In optical waveguides, light travels in a high refractive index medium surrounded by lower index medium. The center region through which the optical rays travel in know as the core, and the surrounding material which imbeds the core is know as the cladding. The light is guided in the high refractive index region due to total multiple internal reflections at the boundaries. In particular, two types of optical devices are important as is shown in Fig.5.10; the optical-fibers and planar waveguides, which are extensively used in optical systems for light transmission and optical and electro-optical devices.

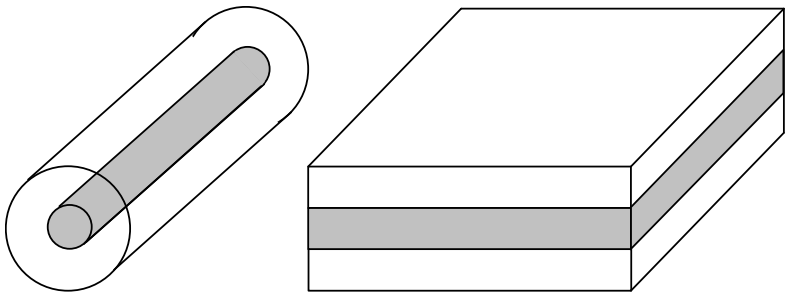


Fig.5.10. Two main types of optical waveguide. a) Fiber. b) Planar waveguide.

5.4.1 Optical fiber.

The development of low-loss optical fiber in the 1970s was a key enabler for the explosive growth of optical communication systems Optical fiber shown in Fig.5.10.a) is a

cylindrical waveguide that consists of a central core surrounded by a cladding layer whose refractive index is lightly lower than that of the core. The energy in fiber is carried partly inside the core and partly outside. The external field decays rapidly to zero in the direction perpendicular to the propagation direction.

Optical fibers may be classified as either single mode or multimode fibers. In the single mode fibers shown in Fig.5.11.a) light can propagate the fundamental mode only. Single-mode fiber allows transmitting a high capacity information because it can retain the fidelity of each light pulse over longer distances, and it exhibits no dispersion caused by multiple modes. Single-mode fiber also enjoys lower fiber attenuation than multimode fiber. Thus, more information can be transmitted per unit of time. However, the smaller core diameter makes coupling light into the core very difficult.

In multimode fibers shown in Fig.5.11.b) and Fig.5.11.c) light can propagate hundreds of modes. This fiber type has a much larger core diameter, compared to single-mode fiber, allowing for the larger number of modes, and multimode fiber is easier to couple than single-mode optical fiber. Multimode fiber may be categorized step-index or graded-index fiber.

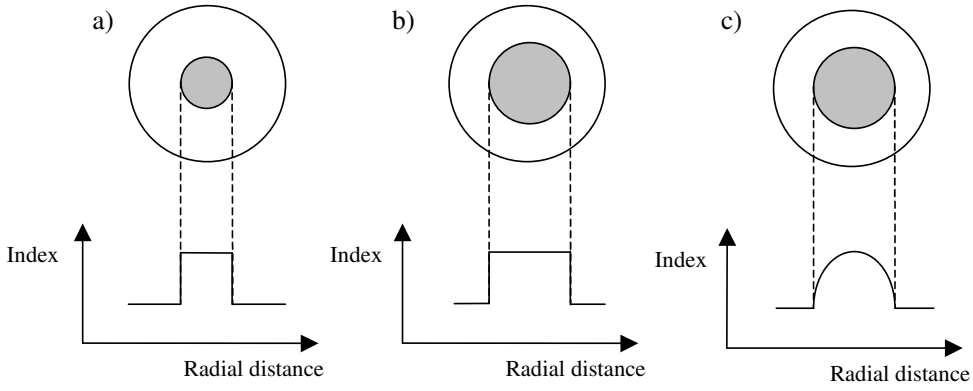


Fig.5.11. The cross-section and the refractive-index profile of optical fibers. a) Single mode step-index fiber. b) Multimode step-index fiber. c) Multimode graded-index fiber.

In a step-index fiber, the refractive index of the core is uniform and undergoes an abrupt change at the core-cladding boundary. Step-index fibers obtain their name from this abrupt change called the step change in refractive index. In graded-index fibers shown in

Fig.5.11.c), the refractive index of the core varies gradually as a function of radial distance from the fiber center.

5.4.2 Planar slab optical waveguide.

Planar optical waveguides are the key devices to construct integrated optical circuits. The simplest structure of planar waveguide is the slab waveguide shown in Fig.5.12. Since, there is no confinement in the horizontal direction, the 'single mode' slab waveguide can't support modes in horizontal direction. Slab waveguide is the ideal infinite planar structure usually used in theoretical analyses of the fundamental properties of dielectric waveguides.

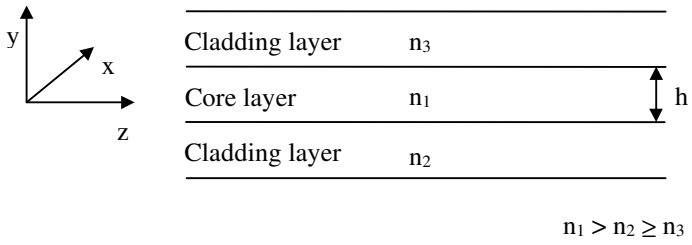


Fig.5.12. 2-D optical slab waveguide.

The light is confined in the core layer by the total internal reflections at the two interfaces and propagates along *z* direction. The propagation constant β along *z* direction exists in the range

$$k_o n_3 < \beta < k_o n_1 \tag{5.10}$$

where k_o is the free-space wavenumber

$$k_o = \frac{2\pi}{\lambda} \tag{5.11}$$

Usually the guided mode is characterized by the effective refractive index, n_{eff}, where:

$$\beta = k_o n_{eff} \tag{5.12}$$

The dispersion characteristics, of guided modes in 2-D slab waveguide with step-index distribution are straightforward derived from Maxwell's equations. The 2-D wave analysis [NIS-00] indicates that pure TE and TM modes can propagate in the waveguide. The TE mode consists of field components E_y, H_x, and H_z, while the TM mode has E_x, H_y, and E_z. A unified treatment of the TE modes is possible by introducing the normalized waveguide propagation constant b and the normalized waveguide frequency V:

$$b = \frac{n_{eff}^2 - n_2^2}{n_1^2 - n_2^2} \tag{5.13}$$

$$V = k_o h \sqrt{;n_1^2 - n_2^2} = \frac{2\pi h}{\lambda} \sqrt{n_1^2 - n_2^2} \tag{5.14}$$

The asymmetric measure of the waveguide is also defined as

$$a = \frac{n_3^2 - n_2^2}{n_1^2 - n_2^2} \tag{5.15}$$

when $n_2 = n_3$, $a = 0$, which implies symmetric waveguide.

By using the above definition, the dispersion equation of the TE_m modes can be expressed in the normalized form

$$V\sqrt{;1 - b} = (m + 1)\pi - \tan^{-1}\sqrt{\frac{1 - b}{b}} - \tan^{-1}\sqrt{\frac{1 - b}{b + a}} \tag{5.16}$$

where m = 0, 1, 2, 3, …is the mode number corresponding to the number of modes in the electric field distribution $E_y(x)$. This equation can be solved numerically. The normalized

dispersion curve is shown in Fig.5.13. The different possible values of b for a given V number correspond to different modes that can propagate in the waveguide. The modes are different possible solutions to the waveguide equations.

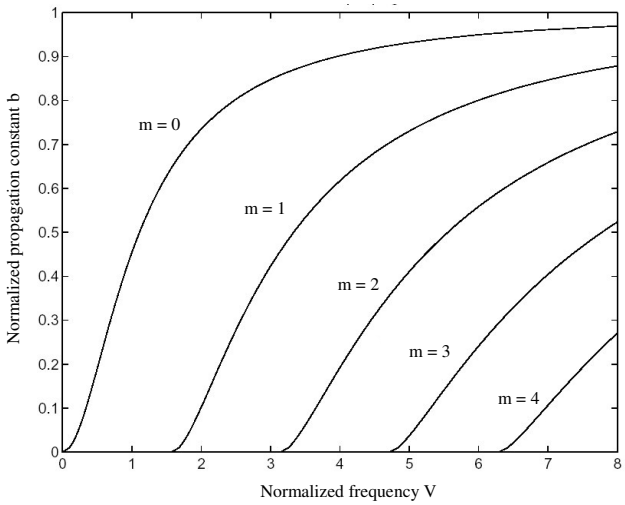


Fig.5.13. Dispersion curves for 2-D symmetrical dielectric slab waveguide.

The symmetric waveguide can always support at least one mode –the lowest order mode. It is possible to obtain an exact condition for a single mode operation by putting the cut-off condition (i.e. b=0) directly into the eigenvalue equation (5.16). Its allow to obtain the range of possible values of V which can support only the lowest order mode in the slab waveguide.

$$\pi + \tan^{-1}\sqrt{;a} > V > \tan^{-1}\sqrt{;a} \qquad (5.17)$$

By substituting the definition for V into (5.17), the condition for single mode waveguide is defined as:

$$\frac{\pi + \tan^{-1}\sqrt{a}}{k_o\sqrt{n_1^2 - n_2^2}} > h > \frac{\tan^{-1}\sqrt{a}}{k_o\sqrt{n_1^2 - n_2^2}} \qquad (5.18)$$

Notice that for the larger refractive index difference the smaller waveguide thickness must be for single mode operation.

One crucial parameter of optical waveguide is the optical confinement factor Γ, which is defined as the fraction of the mode energy which is confined in the core and the total energy in the waveguide. High confinement factor is required to minimize the radiation loss due to the power leaking through the cladding in routing devices such as bend and splitters. The simple expression for estimating the confinement factor in terms of normalized frequency V is given as [BOT-78], [BOT-81].

$$\Gamma \approx \frac{V^2}{2 + V^2} \tag{5.19}$$

A simple application of this equation is to give a crude estimate of the effective refractive index seen by mode.

$$n_{eff} = \sqrt{n_2^2 + \Gamma(n_1^2 - n_2^2)} \tag{5.20}$$

5.4.3 Planar rectangular optical waveguide.

Slab waveguide is the ideal infinite planar structure usually used in theoretical analyses of the dielectric waveguides. In practice, the most common realization of optical waveguide are the rectangular structures presented in Fig.5.14. The propagation behavior of EM waves in rectangular waveguides is very complicated because light is confined in both horizontal and vertical direction.

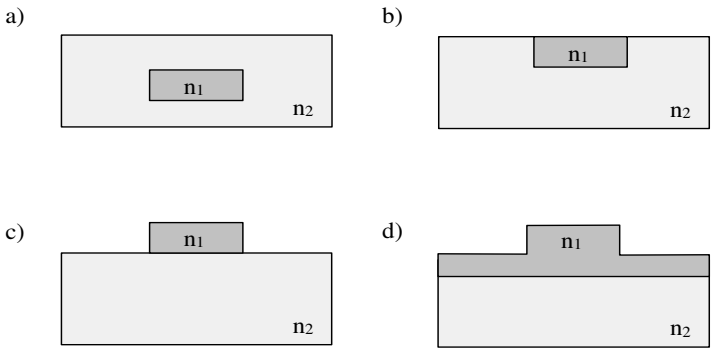


Fig.5.14. Types of rectangular channel waveguides. a) Buried channel. b) Embedded strip. c) Raised strip. d) Rib waveguide.

In order to obtain the fundamental properties of rectangular dielectric waveguides, the effective index method (EIM) [KIM-86], [CHE-90] [NIS-00] is used. By the effective index method a two-dimensional field problem is transformed to a problem for a one-dimensional effective waveguide. This method is usually accurate to better than 0.5%, particularly when the waveguide has aspect ratio (width to height ratio) far from unity. The basic idea of EIM is to approximate the rectangular waveguide with slab waveguides in transverse and lateral directions. In this method the rectangular waveguide shown in Fig.5.15.a) is divided into two 2-D waveguides shown in Fig.5.15.b) and Fig.5.15.c).

First the eigenvalue parameters calculated for the structure shown in Fig.5.15.b) are used to define the effective refractive index n_{eff1} for the core region of the second slab waveguide shown in Fig.5.15.c). A second slab represents the original rectangular waveguide of Fig.5.15.a)

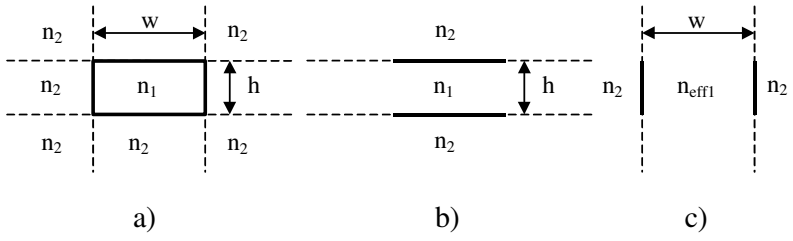


Fig.5.15. Illustration if effective index method.

Most of the waveguide systems built today for fiber optical communication use low Δn, which lead to high bending loss and prevents increasing the packing density. Since sub-micrometer interconnect dimensions and small bending radius are required in IC's applications, the waveguide with high refractive index difference between the core and the claddings must be used. High refractive index difference (Δn) results in very rigid boundaries, thus confining the EM waves very strongly in the waveguide core. To form the planar optical waveguide we assume the use of Si as the core and SiO_2 as the cladding materials. We chose Si/SiO_2 structures because they are compatible with conventional silicon technology and transparent for 1.3-1.55μm wavelength. Such waveguides with high relative refractive index difference between the core (n_1~3.5 for Si) and claddings (n_2~1.5 for SiO_2) allow the realisation of a compact optical circuit, with bend radius of the order of a few μm.

Among various waveguide geometry configurations shown in Fig.5.14., the rectangular strip structure is selected over the others and used in next analysis. This selection was based on the fact that the strip structure more tightly confines the EM field laterally than other structures. This tight lateral confinement with the large Si/SiO_2 refractive index difference, leads to very low bending losses, which allow to realization of a compact optical circuit.

5.5 CONCLUSION.

The optical interconnections are a very attractive solution to solve on-chip global electrical interconnect problems. This chapter has reviewed the optical technology available for implementing the optical communication system. First of all the fundamental difference between optical and electrical signal propagation, which leads to the potential advantage of optical solution was presented. An optical interconnection has at least three parts; transmitter that is a source of optical signal, receiver that is a detector of optical signal, and optical channel that crates a path between them. In order to well understand its properties and interaction all of them have been precisely described.

VI. Optical Clock Distribution Network

Chapter VI

Optical Clock Distribution Network

6.1 INTRODUCTION.

On chip optical interconnects can eliminate most of the problems associated with clock distribution networks in large multigigahertz chips. Optics provides many features such as large bandwidth, low power requirements, reduced crosstalk and better isolation than semiconductor electronics can provide. Many attempts have been recently made to distribute the clock optically. Tewksbury [TEW-97] review many of the approaches which have been explored for optical clock distribution, ranging from the optical clock distribution within lower levels of the system packing hierarchy through optical clock distribution among separate boards of a complex system. Generally there are three main approaches of optical clock distribution: unfocused free-space, focused free-space and guided wave.

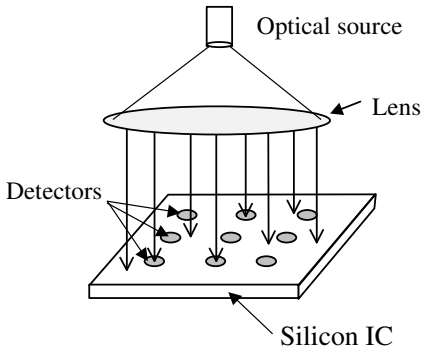


Fig.6.1. General approaches for the unfocused free-space optical clock distribution.

Fig.6.1. presents the main idea of unfocused free-space clock system. In this approach an off-chip source broadcasts to the entire chip, with detectors placed at the desired points. The free-space optical systems provide the flexible distribution with relatively fewer physical contact points on the board region. However, the unfocused system is very inefficient since only a small fraction of the optical energy might be absorbed on the photosensitive areas of the detectors and the rest is wasted. Therefore, inefficient use of optical energy may result in requirements for the extra amplification of the detected signals on the chip.

In the focused free-space optical system shown in Fig.6.2.a) and b) the optical source sent the signal to the desired detector locations through the use of a focusing element, this reducing the need for global masking of the unnecessary regions. The disadvantage of the focused interconnect technique is the very high degree of alignment precision that should be achieved and maintained to ensure that the focused spots are the appropriate places on the chip.

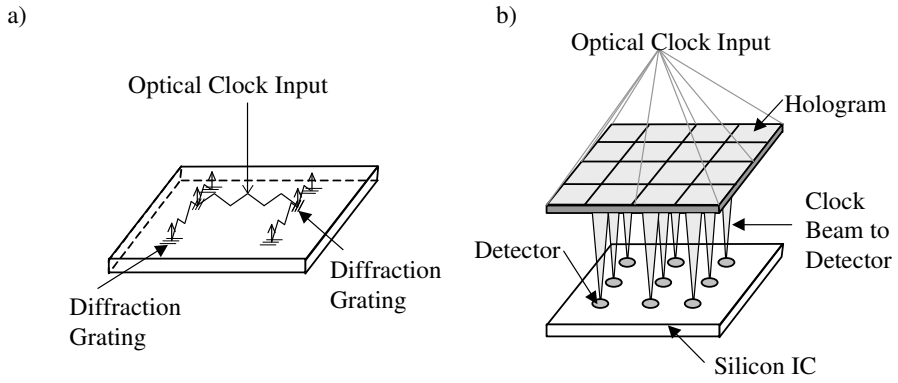


Fig.6.2. General approaches for focused free-space optical clock distribution. a) Substrate-mode guided-wave optical clock. b) Hologram optical clock.

Fig.6.2.a) shows a substrate-mode guided-wave distribution, which represents a compact approach to focused free-space distribution [WAL-92], [TAN-94], [YEH-95], [ZHA-97], and [LUN-97]. In this approach the optical signal is confined within the substrate along the transverse direction. Redirection of the optical signal can occur through multiple gratings, mirrors and microlenses located along individual optical paths.

Fig.6.2.b) presents the focused free-space optical distribution, which employing holographic redirection of the optical signal. There is a many literature on the potential application of holograms for optical interconnections at the integrated circuits and multi chip modules (MCM) levels [BRE-88], [HAU-91], [MOR-2000], [NAK-2002]. Optical clock distribution implementations using holographic optical elements was presented by [KOS-88], [CLY-86] and [LIN-90]. Usually the optical clock signal is applied vertically through use of a hologram. Hologram is the computer generated diffractive optical element designed by an iterative phase retrieval Fourier Transform algorithm. Holograms are similar to binary optics, but whereas binary optics diffracts light due to a surface topology the holographic materials typically contain volumetric features acting as layers of Bragg reflectors.

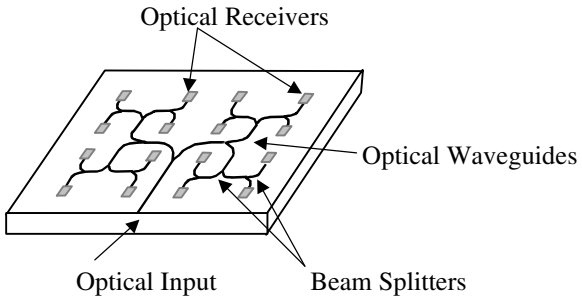


Fig.6.3. General approaches for guided wave optical clock distribution.

Fig.6.3. shows the guided wave system, which based on a net of optical waveguides. The waveguide structures used to optical clock distribution has been recently extensively examined [DEL-91, KOH-94, GIO-98, LI-99, MUL-00, SAM-01, FUK-02]. The optical source is coupled to the symmetrical passive waveguide structure (usually H-tree structure). In the waveguide, light travels in a high refractive index medium surrounded by lower index medium. In particular, two types of optical waveguides are used, multi-mode and mono-mode waveguides. Optical waveguide provides the clock signal to *n*-number of optical receivers, where the high speed optical signal is converted to a logic level electrical signal.

6.2 PROPOSED ARCHITECTURE OF OPTICAL H-TREE.

To provide an unambiguous comparison in terms of dissipated power between the electrical and optical clock distribution networks it is necessary so the optical H-tree network be equivalent to the global electrical H-tree described previously in Chapter 2. To meet this demand the classical approach in describing an n-level electrical H-tree distribution is adopted [BAK-90]. In the proposed system shown in Fig.6.4. a low-power vertical cavity surface emitting laser (VCSEL) is used as an off-chip photonic source. The VCSEL is coupled to the H-tree symmetrical passive waveguide structure and provides the clock signal to *n* optical receivers. The number and placement of the receivers in optical clock system is equivalent to the number and placement of the output nodes in the electrical H-tree. At the receivers, the high speed optical signal is converted to an electrical signal and subsequently distributed by the local electrical networks.

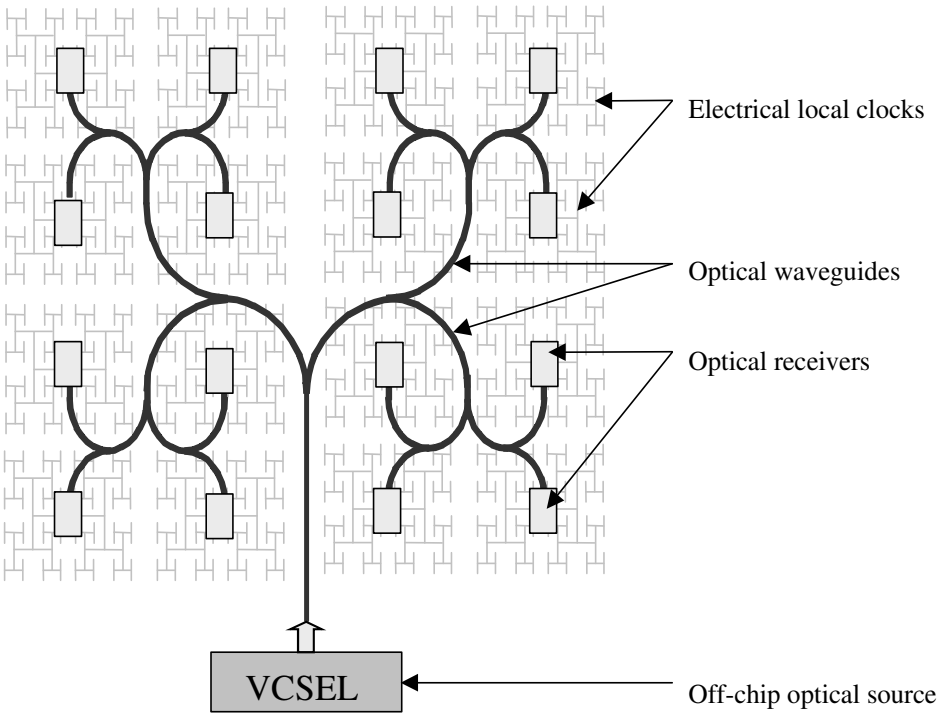


Fig.6.4. General approach to global optical clock distribution network.

Fig.6.5. shows a global optical H-tree optimized for 64 output nodes. To achieve minimal optical losses introduced by the H-tree, the radius of curvatures are designed to be as large as possible. This ensures the smallest distance from source to receivers, which leads to the smallest transmission loss and guarantees a minimal pure bending loss at each curvature. The length of straight segment and the radius of curvature of bend waveguides are associated with the die width, and summarized in Table 6.1. For 20mm die width, the smallest radius of curvature (R6) is 625μm.

Table 6.1. *Curved and straight segment linked to die width.*

Curved segments		Straight segment	
R1	1/8D	d1	3/8D
R2	1/8D	d2	1/16D
R3	1/16D	d3	1/32D
R4	1/16D	d4	1/32D
R5	1/32D		
R5	1/32D		

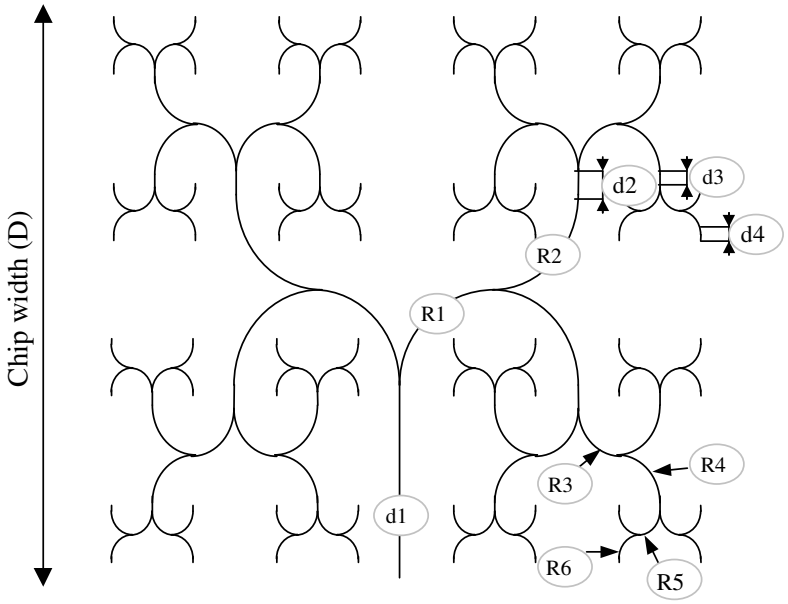


Fig.6.5. Optical H-tree network with 64 output nodes.

To form the planar optical waveguide tree described above, one assumed the use of Si as the core and SiO_2 as the cladding materials, as shown in Fig.6.6. We chose Si/SiO_2 structures because they are compatible with conventional silicon technology and transparent for 1.3-1.55μm wavelength. Additionally, such waveguides with high relative refractive index difference $\Delta \approx (n_1^2 - n_2^2)/2n_1^2$ between the core ($n_1 \approx 3.5$ for Si) and claddings ($n_2 \approx 1.5$ for SiO_2) allow the realization of a compact optical circuit, with bend radius of the order of a few μm.

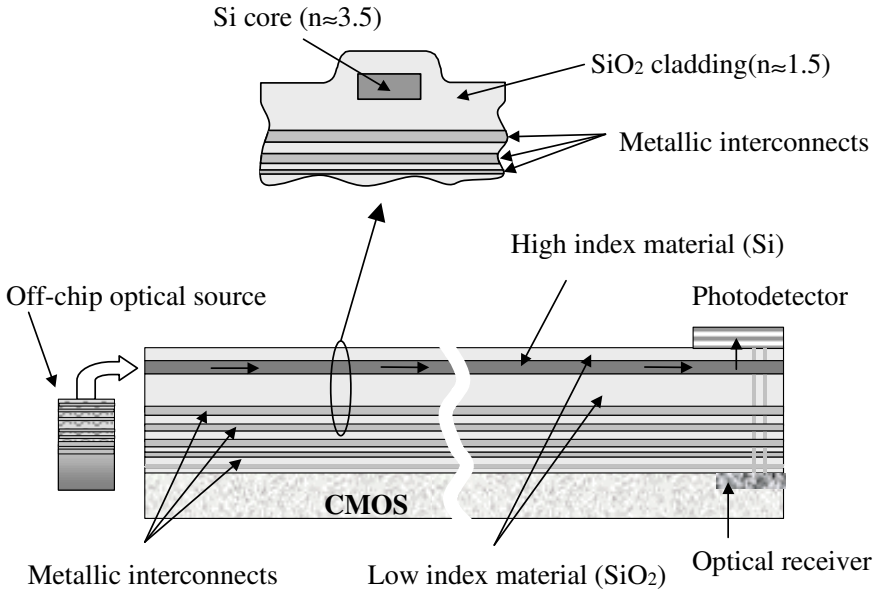


Fig.6.6. Cross section of hybridated interconnection structure.

Among various waveguide geometry configurations, the rectangular strip waveguide structure is selected. This selection was based on the fact that the strip structure more tightly confines the EM field laterally than other structures. To avoid modal dispersion, improve coupling efficiency and reduce losses, single mode conditions are applied to the waveguide dimensions.

6.3 OPTICAL FEATURES DETERMINATION.

In order to properly design the optical H-tree it is necessary to take into account all aspects associated with the optical signal transmission. In particular, the quality of the overall optical system (Bit Error Rate), performance of the optical source and optical receiver and the efficiencies of passive components used in the system. This subchapter described and modeled all these issues in turn.

6.3.1 Bit error rate.

The main criterion in the quality evaluation of the overall digital transmissions systems is the resulting bit errors rate BER [AGR-92], [BRE-03] and it has been also proposed to evaluation the quality of the optical tree design. It is defined as the percentage of bits that have errors relative to the total number of bits received in a transmission. The BER value equal to10^{-6} means that 1 error occurred during the transmission of 10^6 bits. Non zero value of BER results from incorrect decisions being made in a receiver due to the presence of noise on digital signal. Typical BER required by Synchronous Optical NETwork (SONET), Gigabit Ethernet and Fibre Channel specifications is 10^{-10}-10^{-12} or better. In order to ensure sufficient system quality one assumed that for optical clock distribution system BER of 10^{-15} is acceptable.

For unbiased data (number of "1" equals number of "0") bit errors rate can be described as:

$$BER = \frac{1}{2}\,[\,P(0/1) + P(1/0)] \tag{6.1}$$

where P(0/1) is the probability to detect "0" when "1" is transmitted, and P(1/0) is the probability to detect "1" when "0" is transmitted. If we assume that additive white Gaussian noise is dominant cause of erroneous decisions, then the probability density function can be written mathematically as follows:

$$P(0/1) = \frac{1}{\sigma_L\sqrt{2\pi}} \int_{\gamma}^{\infty} \exp[\frac{(V-V_L)^2}{2\sigma_L^2}]dV = \frac{1}{2}\,\mathrm{erfc}\frac{\gamma-V_L}{\sigma_L\sqrt{2}} \tag{6.2}$$

$$P(1/0) = \frac{1}{\sigma_H\sqrt{2\pi}} \int_{-\infty}^{\gamma} \exp[\frac{(V-V_H)^2}{2\sigma_H^2}]dV = \frac{1}{2}\,\mathrm{erfc}\frac{V_H-\gamma}{\sigma_H\sqrt{2}} \tag{6.3}$$

where σ_L and σ_H are the variances corresponding to "0" and "1", V_L and V_H are the signal send by transmitter "0" and "1", respectively, γ is given decision threshold and erfc is well know error function [ABR-70]:

$$\mathrm{erfc} = \frac{2}{\sqrt{\pi}} \int_{x}^{\infty} \exp[-y^2]dy \tag{6.4}$$

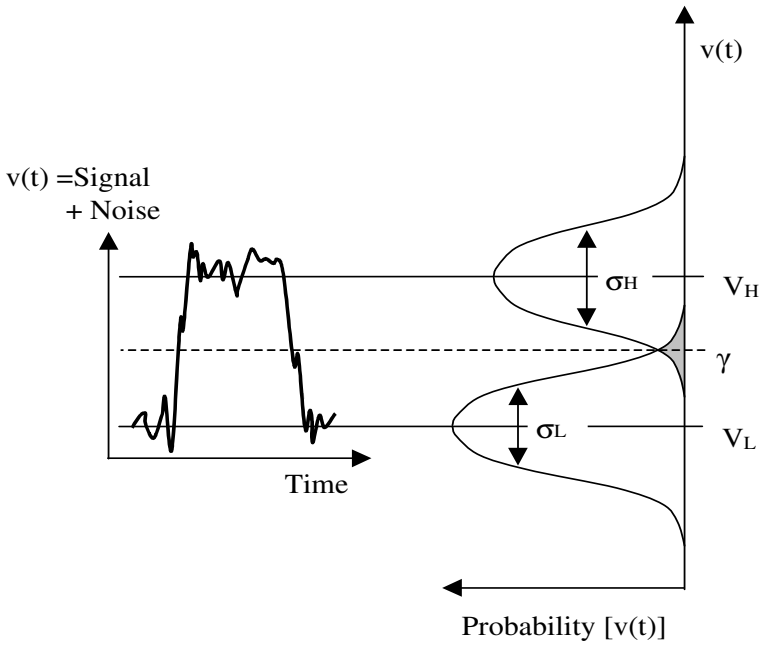


Fig.6.7. Probability of error for binary signaling.

Fig.6.7. and equations (6.1), (6.2), and (6.3) shows that the probability of error is equal to the area under the tails of the density functions that extend beyond decision threshold γ. We can conclude that the BER is determined by the standard deviation of noise (σ_L and σ_H) and the signal difference between V_L and V_H.

By substituting (6.2), (6.3) and (6.4), the BER with the optimum setting of decision threshold is given by:

$$BER = \frac{1}{2}\,\mathrm{erfc}\left(\frac{Q}{\sqrt{2}}\right) \approx \frac{1}{\sqrt{2\pi}}\,\frac{\exp(-Q^2/2)}{Q} \tag{6.5}$$

where Q-factor is given as

$$Q = \frac{V_H - V_L}{\sigma_H + \sigma_L} \tag{6.6}$$

The approximate form of BER is obtained using the asymptotic expansion of erfc($Q/\sqrt{;2}$) and is reasonable accurate for Q > 3. Fig.6.8. shows how the BER varies with the Q parameter.

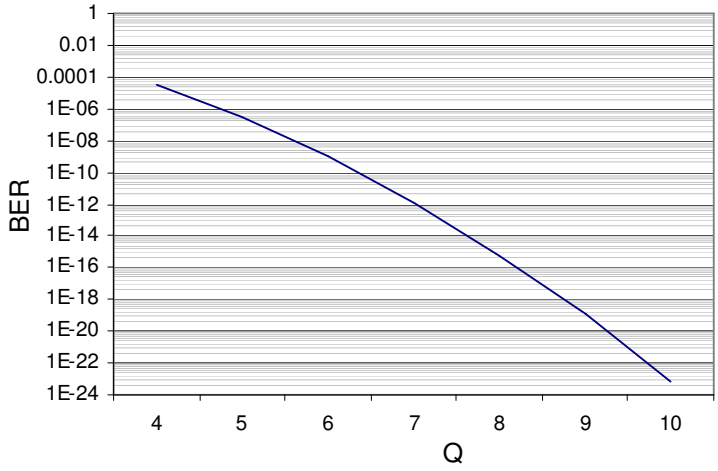


Fig.6.8. Bit error rate (BER) versus the Q parameter.

In the case of an optical transmission line, the Q-factor represents the optical signal-to-noise ratio (SNR) for a binary optical communication system. It combines the separate SNRs associated with the high and low signal levels into overall system SNR. The form of the Q-factor given in equation (6.6) simplifies both the measurement of SNR and the calculation of the theoretical BER due to additive random noise. Assuming V_L equal 0 we obtain:

$$Q = \frac{1}{2}\sqrt{SNR} \tag{6.7}$$

where

$$SNR = \frac{SIGNAL_{(pp)}}{NOISE_{(RMS)}} \tag{6.8}$$

Notice that the signal is in terms of a peak-to-peak signal, whereas the noise is in RMS (average root-mean squared) terms. For example to achieving BER = 10^{-9} one needs Q = 6 and hence SNR = 144 or 21.5dB. It can be concluded that to achieve assumed overall optical system performance (BER) it is necessary to ensure required SNR at the receiver.

6.3.2 Minimal optical power.

The SNR has been used to calculate the minimum optical power that is needs by the receiver to operate with a specified overall system performance. In ideal case (where $P_{"0"} = 0$), the average optical power needed by photodetector is given by a simple expression:

$$P_{AVG} = \frac{1}{2}P_{"1"} = \frac{0.5\sqrt{SNR}\sqrt{i_N^2}}{\Re} = \frac{Q\sqrt{i_N^2}}{\Re} \tag{6.9}$$

where, i_N, is the total noise due to photodiode and the transimpedance amplifier, and $\Re$, is the receiver photo-responsivity: In the reality same power is emitted by most transmitters

even in the "off" state ($P_{"0"} \neq 0$). In the case of semiconductor lasers, the off-state power $P_{"0"}$ depends on the bias voltage and the threshold current. If the laser bias is close to or above the threshold point, $P_{"0"}$ can be a significant fraction of $P_{"1"}$. The ratio of a logic "one" power level ($P_{"1"}$) relative to logic "zero" power level ($P_{"0"}$) is expressed by extinction ratio (r_e):

$$r_e = \frac{P_{"0"}}{P_{"1"}} \tag{6.10}$$

Combining eqns (6.9) and (6.10), the minimum average optical power required by receiver to operate at a given BER is expressed as:

$$P_{AVG} = \left(\frac{1 + r_e}{1 - r_e}\right) \frac{Q\sqrt{\overline{i_N^2}}}{\Re} \tag{6.11}$$

This equation shows that P_{AVG} increases when $r_e \neq 0$. Summary, the minimum average optical power required by each receiver used in the considered clock distribution tree to operate at a given error probability depend on the assumed quality of the overall system, total noise and photo-responsivity of the receiver, and the laser extinction ratio. The minimum average optical power needed by receiver determine the minimal optical power emitted by the optical source.

6.3.3 Loss in passive optical components.

The optical system performance depends on the minimum optical power required by the receiver and on the efficiencies of passive optical components used in the system. The total optical loss in the considered optical clock system is the sum of the losses (in decibels) of all optical components.

$$L_{total} = L_{CV} + L_W + L_B + L_Y + L_{CR} \quad (6.12)$$

where L_{CV} is the coupling loss between the photonic source and optical waveguide, L_W is the rectangular waveguide transmission loss, L_B is the bending loss, L_Y is the Y-spliter loss and L_{CR} is the coupling loss from the waveguide to the optical receiver. All type of these losses are shown schematically in Fig.6.9.

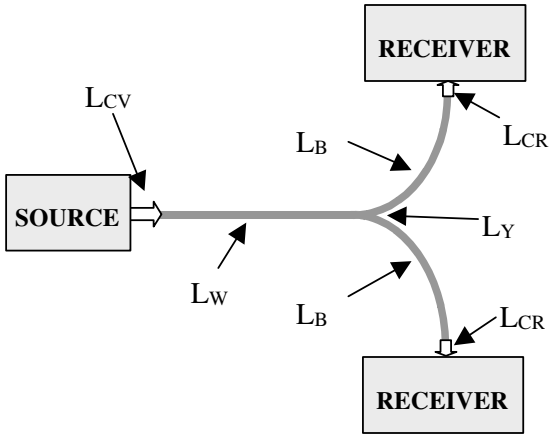


Fig.6.9. Loss sources in optical system.

All of these loss components have been incorporate in the calculation of the optical losses in the proposed optical H-tree clock distribution system.

6.3.3.1 Optical waveguide transmission loss.

Generally, transmission losses can be defined as the attenuation rate of the optical power when light travels in waveguide. The attenuation is the most important figure of merit for optical waveguide systems because it limits the magnitude of transmitted power. It dictates, therefore, the output requirement of the emitter and detection limit of the receiver. Usually, the attenuation coefficient α is defined in the following way:

$$P_{out} = P_{in}e^{-\alpha L} \Rightarrow \alpha = \frac{1}{L}\ln\left(\frac{P_{in}}{P_{out}}\right) \quad (6.13)$$

where P_{in} is the initial value of the power going in the waveguide and P_{out} is the power leaving the waveguide of L length. The transmission losses are usually indicated in decibels (dB) what requires a little change in the equation (6.13) that takes the form:

$$\alpha_T\,[\text{dB/length}] = \frac{10}{L}\log_{10}\left(\frac{P_{in}}{P_{out}}\right) \quad (6.14)$$

The relation between α and α_T can be simple derived from (6.13) and (6.14) and is as follows:

$$\alpha_T\,[\text{dB/length}] \approx 4.343\alpha \quad (6.15)$$

Mechanisms of the waveguide transmission loss

The dominant mechanisms in the optical waveguide are the material absorption, scattering loss and waveguide imperfection loss.

Absorption is related to the waveguide material, and can be divided into two categories: intrinsic material absorption related to the pure waveguide material and extrinsic absorption due to impurities. Optical absorption take place when photon interacts with electrons or with vibrational states of the core. During this interaction the material absorb photons which have sufficient energy to support electronic transition. For the 1.55μm wavelength with 0.8eV energy, the intrinsic material absorption in pure silicon crystal, whose energy gap is ~1.1eV is less then 0.03dB/km. However, any distortion of the crystal lattice order such as random material structure, imperfection, and impurities may give rise to defect states in the energy gap, resulting in the possible extrinsic photon absorption.

The scattering losses, the other major mechanism of waveguide loss, are associated with the local variation of the refractive index on a scale smaller than the optical wavelength λ. Light scattering in such a medium is know as Rayleigh scattering, which is inversely proportional to the λ^4.

$$\alpha_R = \frac{8\pi^3}{3\lambda^4}(n^2\text{-}1)k_B T_f \beta_T) \qquad (6.16)$$

where n is the refractive index, k_B is Boltzmann's constant, β_T is the isothermal compressibility of the material and T_f is the temperature. Rayleigh scattering can be considered to be elastic scattering since the photon energies of the scattered photons is not changed. Scattering in which the scattered photons have either a higher or lower photon energy is called Raman scattering. Usually this kind of scattering involves exciting some vibrational mode of the molecules, giving a lower scattered photon energy, or scattering off an excited vibrational state of a molecule which adds its vibrational energy to the incident photon.

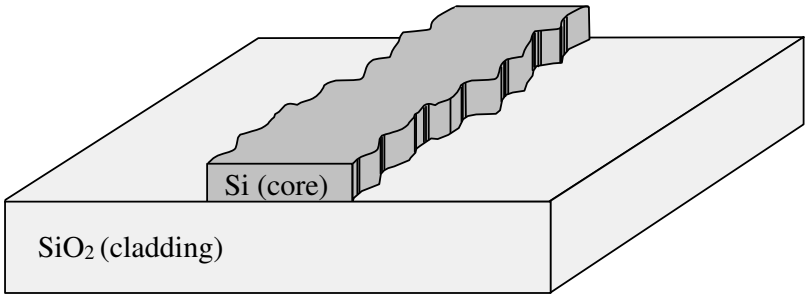


Fig.6.10. Optical waveguide structure after etching process.

The last attenuation mechanisms are the fabrication losses (scattering) resulting from the imperfection in the waveguide geometry. Rectangular strip optical waveguide has four surface which interacts with the guided light, they are the top, botton and sidewall surfaces. Fabrication imperfections of any of these areas can cause significant attenuation due to surface scattering. The surface roughness depends on the technology. Where the first polySi waveguide were fabricated the optical losses were large because of the 25nm rough top surface (and grain boundary) By using the chemical mechanical polishing

(CMP) technology [SEO-03] losses were reduced. The waveguide core height variations are reduced to about 4nm, which is equivalent to perfect flatness. For Si/SiO_2 waveguides its may be assumed that there is negligible roughness loss from both upper and lower core/cladding interfaces. The side-wall roughness is caused by the etching process which is required to form the vertical side-wall like is illustrated in Fig.6.10.

The side-wall scattering is the dominant source of losses in planar optical waveguides. Due to small waveguide dimensions and large index change at the core/cladding interface the optical mode in the waveguide reacts strongly with the side-wall roughness.

The basic scattering theory in the optical waveguides due to side-wall roughness was presented in 1969 by Marcuse [MAR-69]. Author modeled the scattering loss as arising from the coupling between the fundamental guided mode of the waveguide and the radiation modes. Because of its complexity, Marcuse theory requires numerical calculations to achieve the scattering loss. Basing on the Marcuse theoretical work, Payne and Lacey [LAC-90], [PAY-94] formulated, however, a simpler scattering formula using direct calculations of the far field pattern.

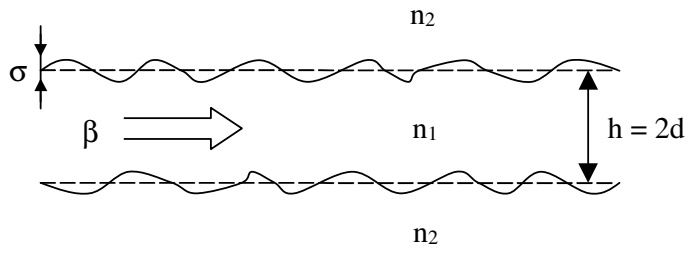


Fig.6.11. Geometry of planar waveguide with random sidewall roughness on two sides.

The complete analytical solution for the scattering loss in the planar optical waveguide with random sidewall roughness σ is given by the combination of the following equations.

$$\alpha = \frac{\sigma^2}{\sqrt{2}\, k_0 d^4 n_1}\, g(V) f_e(x,\gamma) \qquad (6.17)$$

$$g(V) = \frac{U^2V^2}{(1 + W)} \tag{6.18}$$

$$f_e(x,\gamma) = \frac{x\sqrt{\sqrt{(1 + x^2)^2 + 2x^2\gamma^2} + 1 - x^2}}{\sqrt{(1 + x^2)^2 + 2x^2\gamma^2}} \tag{6.19}$$

where k_0 represent the free-space wave number, d is the half of the waveguide width, n_1 is the effective core index, g(V) is the function determined by the waveguide geometry and $f_e(x,\gamma)$ characterizes the integral over the spectral density function described further as:

$$x = W\frac{L_c}{d} \tag{6.20}$$

$$\gamma = \frac{n_2V}{n_1W\sqrt{\Delta}} \tag{6.21}$$

where x represent the normalized correlation length, and γ measures how weakly guiding is the waveguide, L_c is the autocorrelation length described by [LAD-92], [LAD-94], Δ is the relative refractive index difference between the core end the claddings materials, and V, U, W, are the normalized waveguide parameters given as

$$V = \frac{2\pi h}{\lambda}\sqrt{n_1^2 - n_2^2} \tag{6.22}$$

$$U = \frac{2\pi h}{\lambda}\sqrt{n_1^2 - n_{eff}^2} \tag{6.23}$$

$$W = \frac{2\pi h}{\lambda}\sqrt{n_{eff}^2 - n_2^2} \tag{6.24}$$

To apply the Payne formula to a real dielectric waveguide we use the Effective Index Method [KIM-86], [NIS-00], which reduces a 3-dimensional waveguide problem into a 2-dimensional equivalent form. This method has been described in more details in chapter IV.

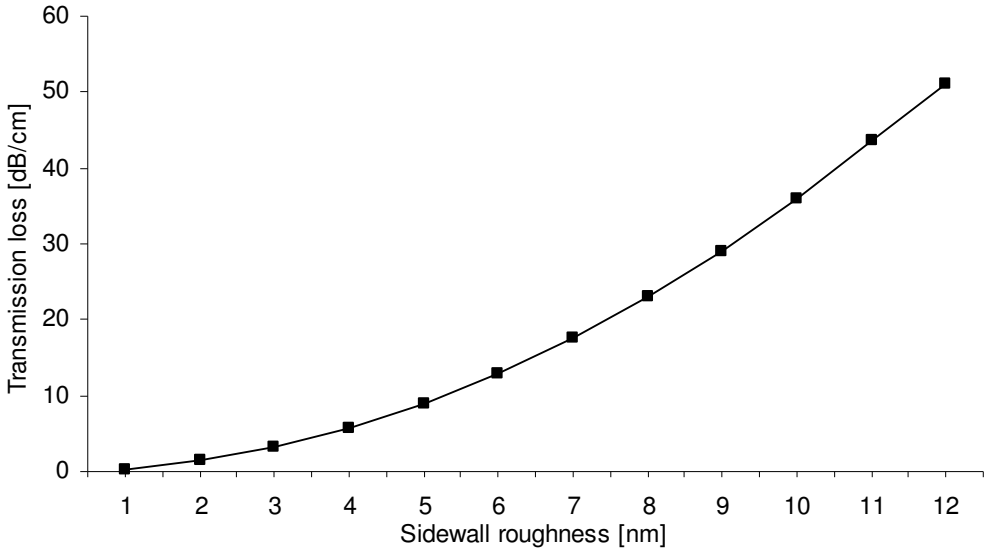


Fig.6.12. Calculated transmission loss of the strip waveguide for various sidewall roughness (waveguide parameters described in Table 7.3 with L_c=50nm).

The calculated transmission loss of the strip waveguide for various sidewall roughness is plotted in Fig.6.12. By using the oxidation smoothing and anisotropic etching method Lee [LEE-01] fabricated the single-mode strip Si/SiO_2 waveguide with sidewall roughness of 2nm The calculated transmission loss for such waveguide is as small as 1.3dB/cm. It should be noted that the measured transmission loss reported by Lee for oxidation smoothing sample is only 0.8dB/cm for 0.05μm waveguide thickness.

6.3.3.2 Optical waveguide bending loss.

The bending loss has been the subject of many research works. The nature of radiation from bent waveguide was first reported by [MAR-69], his analysis is based on a

solution of the eigenvalue equation of the curved waveguide. The bending loss is caused by the phase mismatch between electric field in the core and electric field in the cladding. Since the outer cladding is unable to support the required electric field at the velocity of propagation, the power is radiated from the core as it is intuitive illustrated in Fig.6.13.a). The bend waveguide with radius R_c behaves like straight waveguide with the refractive index profile shown in Fig.6.13.b).

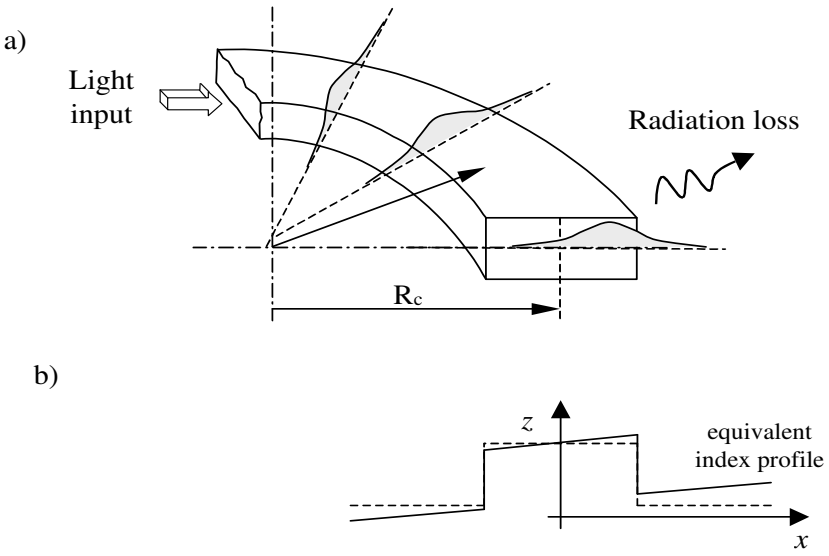


Fig.6.13. Schematic view of: a) Modal propagation in a bent. b) Equivalent index profile

Marcuse [MAR-71], [MAR-73] used a perturbation method to solve the bending loss problem and showed that his results were numerically similar to those obtained by Marcatili. To obtain the bending loss L_B we use the Marcuse method:

$$L_B = \frac{2\,\gamma\kappa^2 e^{2\gamma d} e^{-U}}{(n_1^2-n_2^2)/k_0^2\beta(2d+\frac{1}{\gamma}+\frac{1}{\theta})} \tag{6.25}$$

where

$$U \approx \frac{2}{3}\frac{\gamma^2}{\beta^2}\gamma R_c \tag{6.26}$$

where γ, κ and θ are the waveguide eigenvalues, β is the propagation constant and R_c is the radius of curvature. The obvious consequence of (6.26) is that the bending loss is an exponential function of the curvature and that the bending loss L_B is highly dependent on the refractive index difference between core and cladding medium. In the lower-Δ waveguides, the bending loss was as high as 3dB for radius of curvature as large as 15mm. This prevents increasing the packing density. Since sub-micrometer interconnect dimensions and small bending radius are required in IC's applications, the waveguide with high refractive index difference between the core and the claddings must be used. Some device using dielectric waveguide with high refractive index difference (Δn) have been reported in [SEK-89], [SUZ-94]. High-Δ results in very rigid boundaries, thus confining the EM waves very strongly in the waveguide core. Due to the strong optical confinement, the bend radius as small as a few μm may be realized [SAK-01].

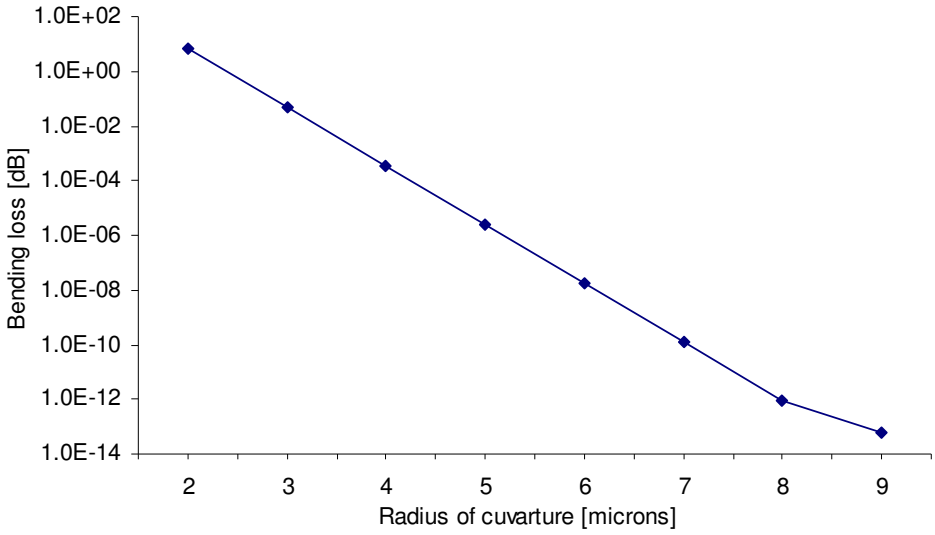


Fig.6.14. Simulated bending loss for Si/SiO_2 strip waveguide. (waveguide parameters described in Table 7.3).

Fig.6.14. shows the simulated bending loss of single mode Si/SiO_2 strip waveguide. As can be seen from this figure, the pure bending losses associated with high-Δ waveguide are negligible if the radius of curvature is bigger then 2μm.

6.3.3.3 Y-splitter loss.

The Y-splitter is a common structure used in integrated optical system. These structures can be used as power dividers; switches, and mode converters. The Y-splitter loss L_Y depends on the reflection and scattering attenuation into the propagation path and surrounding medium. Different Y-splitter structures have been analyzed by several methods [KUZ-85], [RAN-89], [CHU-92]. The data primarily addresses low-Δ optical system, which suffer severe radiation losses at angles greater than 2°-3°.

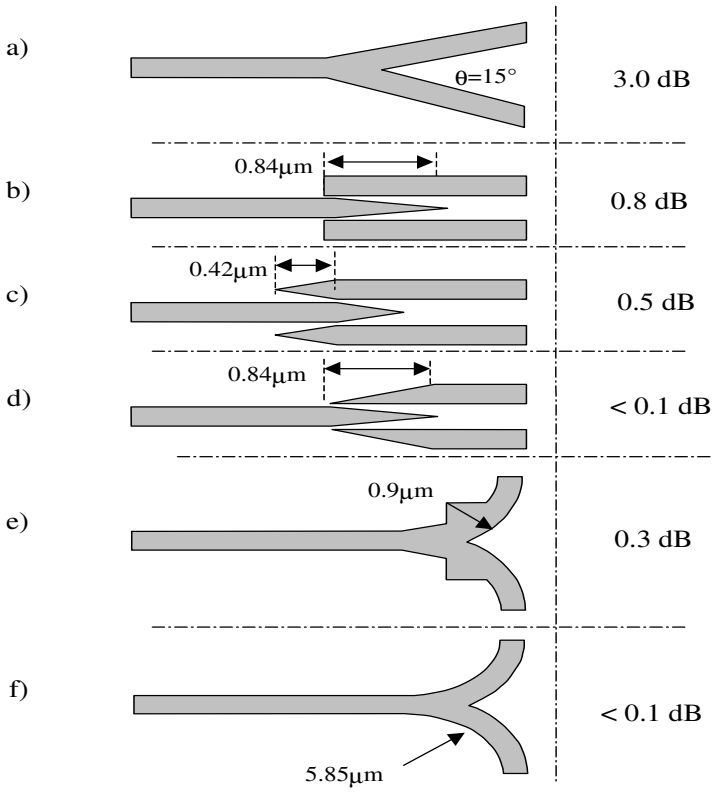


Fig.6.15. Various branch structures.

For high refractive index difference waveguides the losses for the Y-branch are significantly smaller then for the low-Δ structures, Sakai [SAK-02] studied various branches structures as shown Fig.6.15. Among these structures, the modified antenna-coupled-type shown in Fig.6.15.d) and bend-waveguide type shown in Fig.6.15.f) represent loss smaller than 0.1dB per splitter.

6.3.3.4 Input, output coupling loss.

An important issue in any optoelectronics waveguide systems is the coupling between the waveguide transmission part and the light emitting and receiving electronics elements. Such elements have been also distinguished in Fig.6.9, and the appropriate power losses, L_{CV} and L_{CR}, have been attributed to their interface with the waveguide on chip. The origin of these losses results from the imperfect contact between the light conducting materials on the both side of the interface and from the geometrical mismatch due to not all power emitted at one side of the interface can be collected and transferred further at the opposite one. It means that the magnitude of these losses depend on the quality of the interface and can be equal zero if the technology of interface manufacturing is perfect.

It has been assumed that the laser supporting the optical H-tree shown in Fig.6.4 is out of the chip and the light signal is delivered to the planar waveguide on the chip by an external single mode fiber that is ideally coupled with the laser by the laser manufacturer and the losses at this interface are equal to zero. At present stage of technology, one can distinguish several methods to couple the beam emitted from the laser's fiber into optical planar waveguide, like the butt-end coupling, lens and microlens coupling [KAR-90], [GAN-98] or tapered fiber coupling [MAR-88] as is illustrated in Fig.6.16.

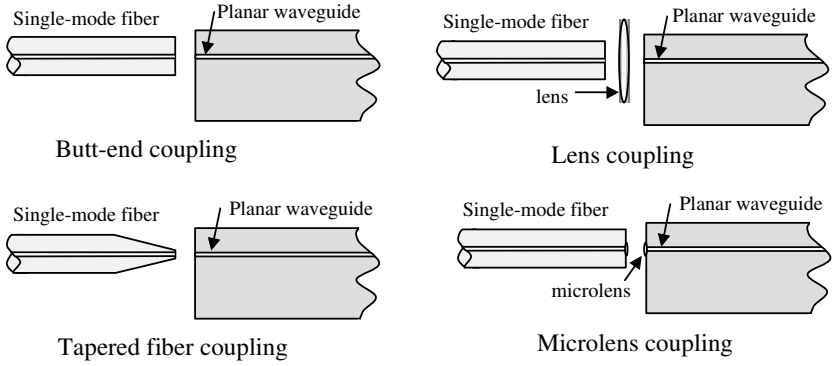


Fig.6.16. Various coupling structures.

The methods shown in Fig.6.16. are costly and very inconvenient from the packing point of view and only one such a coupling is considered in the optical H-tree design (from optical source to planar waveguide). The waveguide grating or waveguide mirror based couplers that are shown in Fig.6.17. are proposed to overcome this problem and these solutions are considered as the proposal for the on chip output coupling. The volume grating coupler for coupling light into an optical receivers from optical waveguide is presented in [SCH-98,SCH-00,MUL-01], and the authors of [MUL-01] reported 86.5% coupling efficiency of their design. This method allows realizing an effective output coupling, but requires precise control of grating parameters. In [GAN-99,LIU-01], the 45° total interior reflection (TIR) micromirror fabricated within the channel waveguide is presented, which estimated output coupling efficiency was nearly 100% for 850nm wavelength.

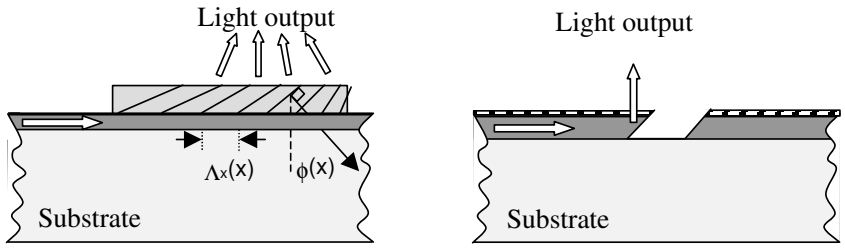


Fig.6.17. Schematic view of the waveguide grating and waveguide mirror based couplers.

One can conclude that using currently available materials and methods it is possible to achieve high input/output coupling efficiency in any presented above solutions. However, this technology is not yet mature, although the research progress in recent years has been substantial. Taking that in mind, in the considered clock distribution system, a more conservative assumption has been made that the input coupling efficiencies L_{CV} and L_{CR} were equal at least to 50% and 87%, respectively.

6.4 CONCLUSION.

This chapter deals with the design of an optimum optical H-tree clock distribution network. In order to H-tree network be equivalent to the global electrical H-tree described previously in Chapter 3 the classical approach in describing an n-level electrical H-tree distribution have been adopted. In the proposed system a low-power VCSEL is used as an off-chip photonic source. The VCSEL is coupled into H-tree symmetrical waveguide structure and provides the clock signal to *n* optical receivers. At the receivers, the high speed optical signal is converted to an electrical signal and subsequently distributed by the local electrical networks. The methodology and the assumptions used to properly design the optical H-tree are presented. In particular for the given quality of the overall optical system, performance of the optical source, optical receiver and the efficiencies of passive components used in the system have been determined.

VII. Optical versus Electrical Clock System

Chapter VII

Optical versus Electrical Clock System

7.1 INTRODUCTION.

Optical interconnections, which are a very attractive solution to solve on-chip global electrical interconnect problems, can also be used in clock distribution systems. However, before an optical clock distribution network can become a reality, the cost versus performance trade-off must clearly favor such a paradigm shift. To provide an unambiguous comparison in terms of power loss between the optical and electrical clock distribution networks, it is necessary to estimate the electrical power consumption in both systems. Since the H-tree architecture is the most representative structure used in classical clock distribution system, the electrical and optical clock distribution using such an architecture have been chosen for modeling. They were numerical investigations of the electrical and optical global H-tree clock systems aimed at the evaluation of their features as well as the comparison of both solutions in terms of dissipated power for future technology generations.

7.2 ELECTRICAL CLOCK DISTRIBUTION NETWORK.

In classical technology, the global clock distribution network that covers the longest lines is routed on the upper metallization layers and distributes the clock signal to the centres of the secondary balanced clock trees using a buffered H-tree architecture. The power dissipation in the electrical clock system is attributed to the charging and

discharging of the parasitic wiring and buffer capacitances, and to the static power dissipated in the buffers, as described in Chapter 3. In order to calculate this power dissipation, a simulator called ICAL, which allows the modelling and calculation of the electrical parameters of clock networks for present and future technology nodes has been developed and was presented in Chapter 4.

Table 7.1 *Microprocessor technology features.*

Technology [nm]	130	100	70	45
T_{ox} [nm]	3.3	2.5	1.6	1.4
Supply voltage [V]	1.2	1	0.9	0.6
Chip size [mm^2]	300	300	400	450
Number of metal levels	7	8	10	10
Total interconnect length [m/cm^2]	4086	5788	11169	15063
Dielectric constant	3.6	3.3	3	2.7
Global wiring A/R (for Cu)	2	2.1	2.2	2.3
Global wiring minimum pitch [nm]	670	475	320	205
Minimal wire width [nm]	335	237	160	103
Minimal wire thickness [nm]	670	500	352	235
Optimal wire width [nm]	1250	1005	850	620
Optimal wire thickness [nm]	2500	2110	1870	1426

The first input to the ICAL program is the set of technology parameters for the process of interest, in particular the feature size, dielectric constant and metal resistivity according to the ITRS roadmap. These parameters for various technology nodes are presented in Table 7.1. Since the interconnect cross-section dimensions affect several system parameters (delay, area, power etc.) it is necessary to determine these values accurately. The optimal global interconnect width for each technology node, which results in small interconnect delay as well as high interconnect density, and has large bisectional bandwidth, is obtained based on the ITRS parameters and the methods presented in [NAE-01], [NAE-02], [VEN-03]. The optimal global wire width and thickness used in global clock network modeling for each technology node are summarized in Table 7.1.

For such interconnect dimensions, using the analytical models and formulas described in Chapter 4, ICAL proceeds to calculate the resistance, capacitance and inductance for a given wire. In the next step, based on the analytical formulas and the BSIM transistor models [BSIM] ICAL calculates the input capacitance and output resistance of the minimal size inverters. The detailed electrical CDN parameters calculated by ICAL for data collected in Table 7.1 are summarised in Table 7.2.

Table 7.2. *Electrical CDN system performance.*

Technology	nm	130	100	70	45
Buffer output resistance (min. size inv.)	kΩ	3.94	4.95	8.02	15.7
Buffer input capacitance (min. size inv.)	fF	0.77	0.66	0.457	0.34
Wire resistance (min. pitch)	Ω/mm	98	186	391	909
Wire capacitance (min. pitch)	F/mm	2.43E-13	2.27E-13	2.10E-13	1.92E-13
Wire inductance (min. pitch)	H/mm	3.2E-10	3.2E-10	3.20E-10	3.2E-10
Wire resistance (optimal width)	Ω/mm	7.04	10.04	13.8	24.9
Wire capacitance (optimal width)	F/mm	3.4E-13	3.11E-13	2.92E-13	2.64E-13
Wire inductance (optimal width)	H/mm	2.13E-10	2.18E-10	2.11E-10	2.14E-10
Opt. segment length (optimal width)	mm	2.88	2.16	1.67	1.32
Optimal buffer size (optimal width)	μm	322	354	496	648

Once the electrical parameters of the CDN have been determined, the required number and size of buffers needed to drive the clock network can be determined. This can be done based on the RC or RLC buffer insertion methods described in Chapter 4. Since the inductance starts to become significant for long metal interconnections and high frequency operation, the RLC method has been chosen for further investigations. Based on the data presented above, the most important calculations (particularly the number and size of the buffers, the total number of transistors, their area and the power dissipated in the clock system for considered technology nodes) are plotted in Fig.7.1-7.4.

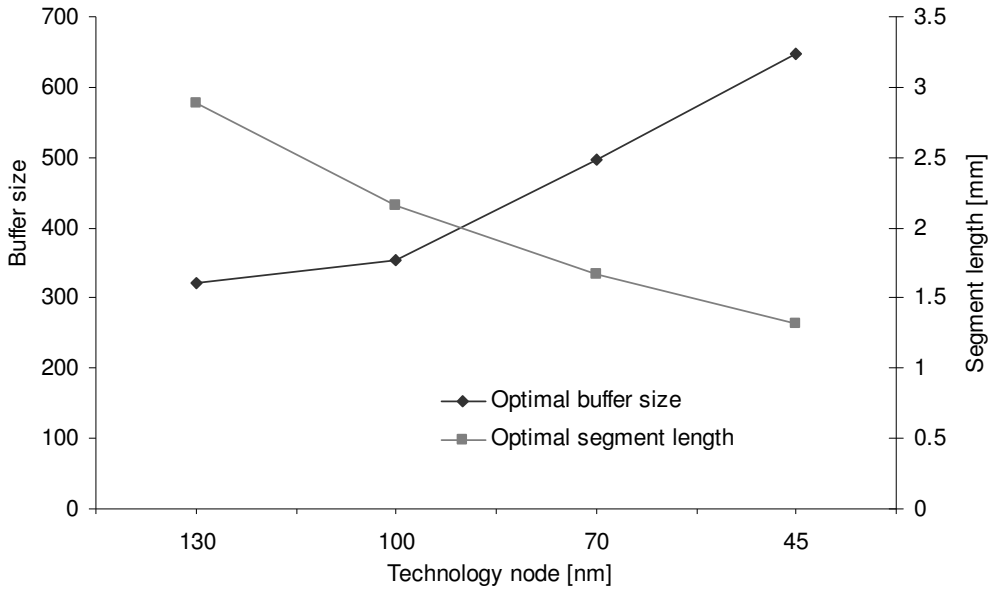


Fig.7.1. Optimal buffer size and optimal segment length estimated vs. technology node.

Fig.7.1 shows the optimal buffer size and optimal segment length estimated from the RLC buffer insertion method for various technology nodes. It is clear from this figure that the required size of the repeater increases with decreasing feature size, whereas the optimal segment length decreases. This goes to show that in future technologies, global interconnects require an increasingly large number of repeaters, which leads to growth in circuit complexity and consequently the power consumption.

Fig.7.2 shows the total number of transistors used in the 128 and 256 nodes H-trees clock networks and their area for considered technology nodes. While the total amount of transistors is larger, their occupied area decreases. This can be explained by the higher integration density in future technology nodes.

Once the optimal buffer size and optimal segment length have been determined, based on the regularity of the H-tree structure, ICAL creates the SPICE netlist where the interconnects are replaced by RC or RLC distributed lines coupled by buffers designed as CMOS inverters. To simulate repeaters, the Berkeley BSIM3v3 models for the 130nm, 100nm and 70nm nodes, and BSIM4 model for the 45nm node were used. The power dissipated in the system can be extracted from transistor-level simulations or from the analytical calculations with an acceptable degree of accuracy.

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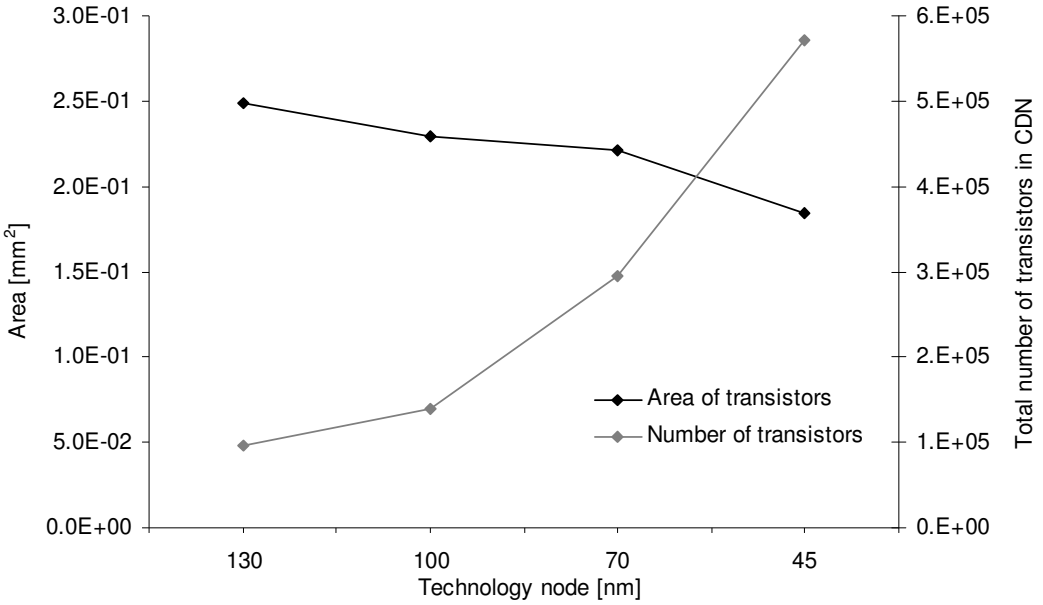

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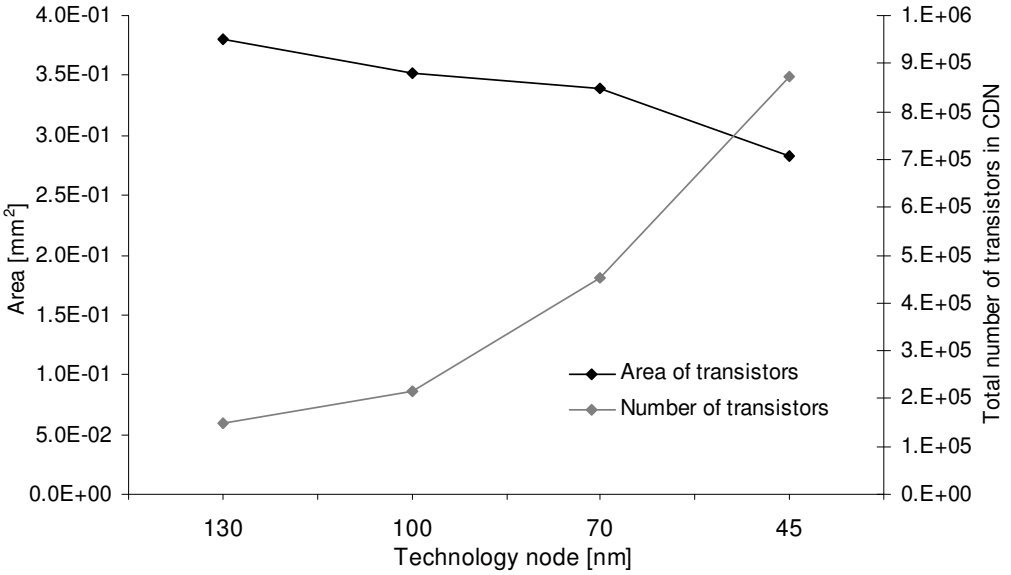
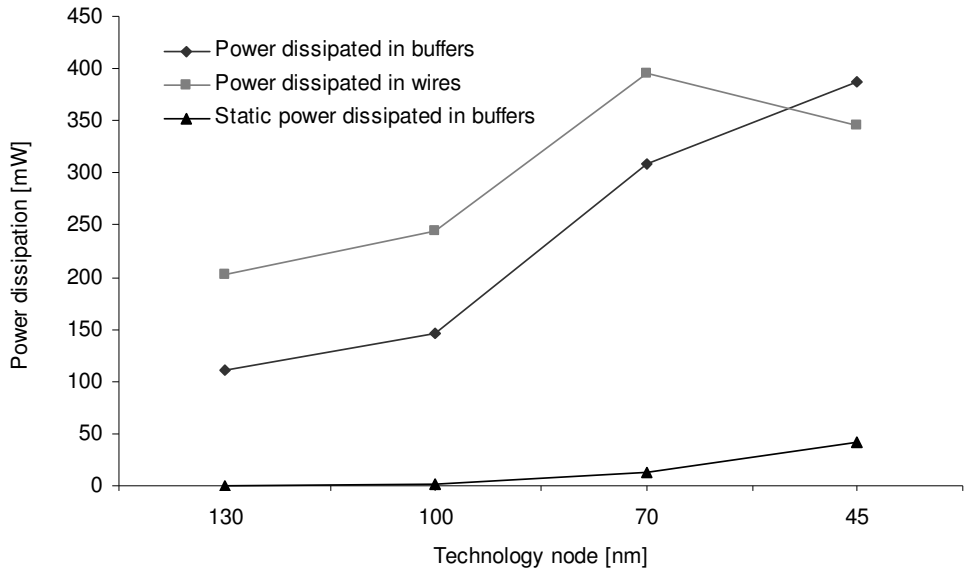


Fig.7.2. Total number of transistors used in CDN and their occupied area vs. technology node. a) 128 output nodes b) 256 output nodes.

a)



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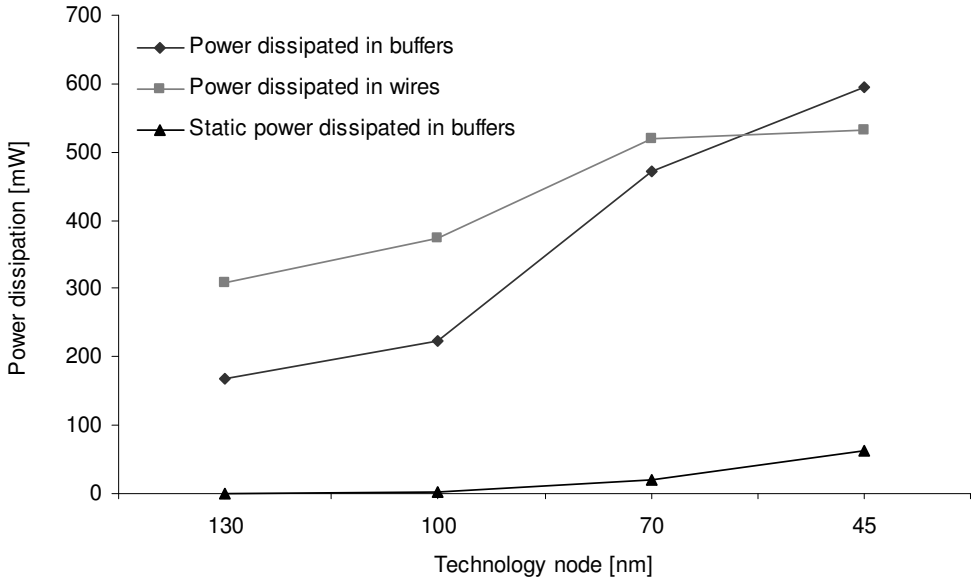


Fig.7.3. Power budget in the electrical H-tree networks. a) 128 output nodes b) 256 output nodes.

Fig.7.3 shows the power dissipated by buffers and wires in 128 and 256 output node H-tree networks for various technology nodes. It is clear from this figure that along with technology scaling the contribution of the power consumed by buffers to the total

power consumption tends to grow, and for the 45nm technology will be even bigger than the power consumed by wires. It is caused by the increasingly large number of repeaters used in clock distribution systems and by the increasing static power dissipation. While dynamic power is partially offset by the reduction of supply voltage that occurs during scaling, static power is increasing exponentially as the threshold voltage decreases. Projecting this trend forward, the static power dissipation due to subthreshold leakage will become an important component of total power dissipation.

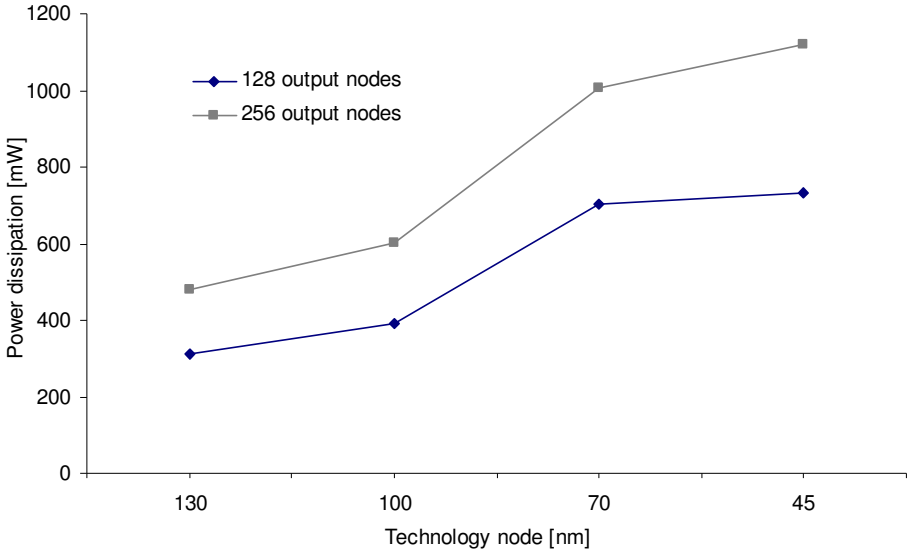


Fig.7.4. Power dissipated in electrical H-tree networks vs. technology

Fig.7.4. shows the calculated electrical power consumption in the global H-trees with 256 and 128 output pins respectively versus technology node. It is assumed that according to the ITRS prediction the operating frequency for considered systems are 1.6GHz for the 130nm node, 3GHz for the 100nm node and 5.6GHz and 11.5GHz for the 70nm and 45nm nodes respectively. It is obvious from this figure that the total power consumption in electrical clock distribution network tends to grow despite technology improvements. The most significant contributor to energy consumption is the average dynamic power dissipation (fCV^2). Since both operating frequency and the switched load associated with parasitic capacitance are increasing one can observe an almost linear increase of the power consumption.

7.3 OPTICAL CLOCK DISTRIBUTION NETWORK.

It was assumed in the previous section that the electrical global clock distribution network distributes the clock signal to the centres of secondary balanced clock trees using a buffered H-tree architecture. To provide an unambiguous comparison between the electrical and optical clock distribution network both the systems should be equivalent. To meet this demand the classical approach in describing an *n*-node electrical H-tree distribution is adopted in the case of the optical system. Its architecture is shown in Fig.6.4. It comprises a low-power vertical cavity surface emitting laser (VCSEL) used as an off-chip photonic source [AMA-02] that is coupled to the symmetrical passive waveguide structure (Si/SiO_2) and provides the clock signal to *n* optical receivers. The incoming optical signal is converted into an electrical signal by the photoreceiver that consists of an InGaAs PIN photodiode [HAM] and a transimpedance amplifier [TIS-03].

Table 7.3. *Optical system performance.*

Optical system performance		
Wavelength λ	μm	1.55
Waveguide core index (Si)	-	3.475
Waveguide cladding index (SiO_2)	-	1.444
Waveguide thickness	μm	0.2
Waveguide width	μm	0.5
Waveguide roughness [LEE-01]	nm	2
Transmission loss	dB/cm	1.44
Loss per Y-junction [SAK-02]	dB	0.2
Input coupling coefficient	%	50
Output coupling coefficient	%	87
Bit error rate (BER)	-	10^{-15}
Photodiode capacitance [HAM]	fF	100
Photodiode responsivity [HAM]	A/W	0.95
VCSEL threshold current [AMA-02]	mA	1.0

The power dissipated in the optical global CDN has been calculated based on the system performance summarised in Table 7.3. These data are also used as the basic set for any further consideration aimed at evaluation of its impact on optical system behaviour.

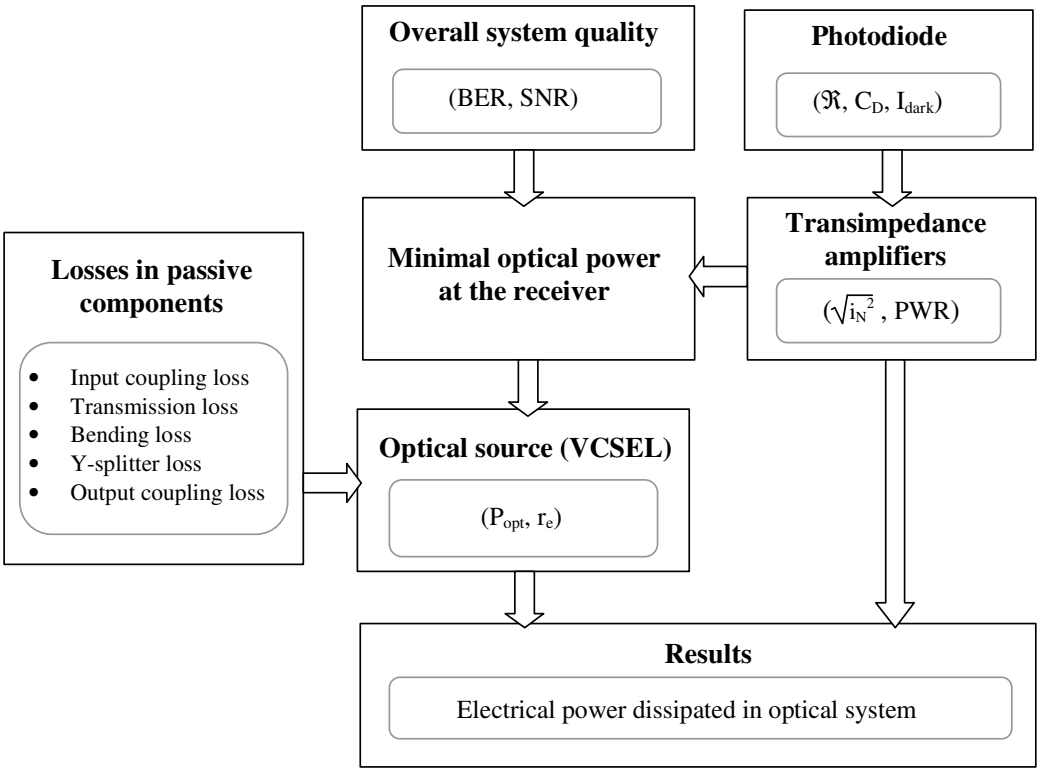


Fig.7.5. The flow diagram of the methodology used in OPTO-ICAL software.

In the optical clock distribution network, there are two main sources of electrical power dissipation. The first is the power dissipation associated with the optical receivers, and the second is the energy needed by the optical source to provide the required optical output power. In order to allow the calculation of the electrical power dissipation in the optical CDN, based on the considerations presented in Chapter 6, the software package called OPTO-ICAL has been developed. Its flow diagram presenting the applied methodology of power estimation is shown in Fig.7.5. First, the required transimpedance amplifier is designed based on given photodiode parameters (C_D,R,I_{dark}), and on a frequential analysis of structures and a mapping of the component values to coefficients in filter approximation function of Butterworth type [CON-02], [TIS-03]. This method gives a maximum bandwidth/power ratio. Next, for a given system performance (BER) and the

noise signal associated with the photodiode and the transimpedance amplifier circuit, the minimal optical power required by the receiver to operate at the given error probability is calculated. To estimate the optical power emitted by the VCSEL, OPTO-ICAL takes into account the minimal value of the signal required by the receiver and the losses incurred throughout all passive optical components. The power dissipated in the optical clock network is the sum of the power dissipated by *n*-number of optical receivers and the power needed by the VCSEL to provide the required optical power to the receivers. The electrical power dissipated by the receivers is extracted by OPTO-ICAL from transistor-level simulations. To estimate the energy needed by the optical source, the laser light-current characteristics shown in Fig.7.6. [AMA-02] were used.

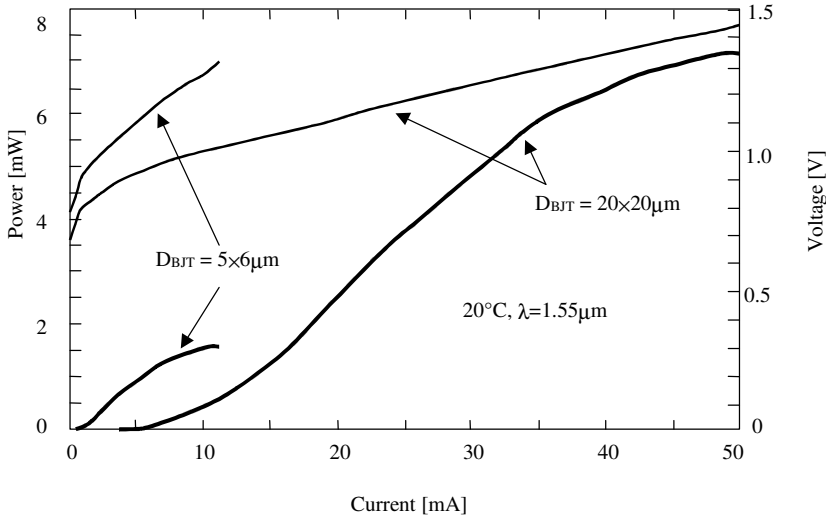


Fig.7.6. Optical output power (thick curves) and voltage (thin curves) versus current for two different dimensions VCSEL structures [AMA-02].

The OPTO-ICAL package has been used to evaluate the features of the global H-tree covering a different number of output nodes from a small number to 256. This figure is supposed to be the largest one for a typical global H-tree clock system. There are several optical components that can influence the overall optical clock distribution system quality such as the optical waveguide quality, which determines the transmission loss, input/output coupling system etc. Their technology is not yet mature and one can expect that their features will improve according to progress in technology of their fabrication. In order to

evaluate how the changes of particular components features will influence the feature of the whole optical H-tree, appropriate simulations have been performed for the global H-tree covering 128 and 256 output nodes, respectively. These results are presented in Fig.7.7 – 7.11. The electronic elements used in the receiver have been treated as designed according to 70nm technology node rules and the operating frequency has been assumed as equal to 5.6 GHz, according to ITRS predictions. The optical power budgets corresponding to H-tree designs on 20x20mm^2 silicon dice are summarised in Table 7.4. They cover the power losses corresponding to the particular elements of the optical waveguide, the Y-dividers multiplication factor representing the power distribution at each waveguide splitter and the total optical losses in the elements making up the H-tree lines. As additional data, the minimum optical input power required by one receiver and the required optical output power of the supplying VCSEL have also been presented. The variations in electrical power consumption by both receivers and VCSEL are shown in Fig.7.7.

Table 7.4. *Optical power budget for 20mm die width at 5.6GHz operating frequency.*

Number of nodes in H-tree		4	8	16	32	64	128	256
Transmission loss in straight	dB	1.44	1.44	1.44	1.44	1.44	1.44	2.16
Transmission loss in curved lines	dB	1.13	1.41	1.7	1.84	1.98	2.05	1.56
Y-dividers multiplication factor	dB	6	9	12	15	18	21	24
Loss in Y-splitters	dB	0.4	0.6	0.8	1	1.2	1.4	1.6
Output coupling loss	dB	0.6	0.6	0.6	0.6	0.6	0.6	0.6
Input coupling loss	dB	3	3	3	3	3	3	3
Total optical system loss	dB	12.6	16.1	19.6	22.9	26.2	29.5	32.9
Min. power at the receiver	dBm	-23	-23	-23	-23	-23	-23	-23
VCSEL optical output power	mW	0.095	0.204	0.45	0.97	2.09	4.46	9.76

Considering the data in Table 7.4, it can be noticed that, for an H-tree of 4 to 128 nodes, the losses in straight lines are equal to 1.44dB/cm. This is caused by the fact that in the optimised optical H-tree the radii of curvature of bend segments are designed to be as large as possible, so that the total length of the straight segments in such a tree is equal to half the chip width. In the case of 256 (or more) output node H-trees, the radius of curvature of the first (and subsequent, depending on the total number of nodes) bend

segments needs to be smaller than optimal in order to avoid intersections that lead to the increase in the total length of the straight segments.

The curves plotted in Fig.7.7 shows the electrical power dissipated by the VCSEL and by the receivers for various H-tree nodes. It can be seen from this figure that for a small number of nodes in the H-tree, the power consumed by the VCSEL is comparable to the power consumed by receivers, but along with the increasing number of nodes, the power consumption in the receivers tends to dominate the total electric power consumption.

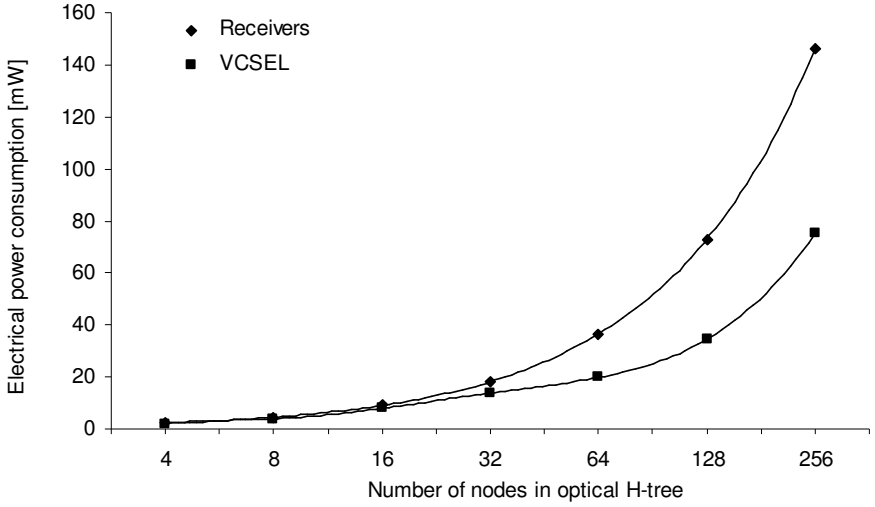


Fig.7.7. Electrical power consumption by the VCSEL and receivers .

In Fig.7.8 the dependence of the optical power emitted by the VCSEL necessary to provide a given system quality on waveguide transmission losses are shown. It is clear from the figure that the transmission losses introduced by the waveguide structure have significant influence on the required optical power emitted by the VCSEL, which affects the total power dissipated in the optical clock system. Comparing Fig.7.8 with Fig.6.12 leads to the conclusion that a small change in the waveguide performance (for example from 2 to 5.5nm sidewall roughness) will result in the enormous change in the laser optical power that needs to be provided. For example, according to Lee [LEE-01], in the case of 128 H-tree output nodes, 1.44dB/cm waveguide transmission losses are achieved for 2nm sidewall roughness, which requires 4.6mW of the optical power emitted by VCSEL,

whereas for 5.5nm sidewall roughness the transmission losses are 10dB/cm and the required VCSEL optical power is 558mW.

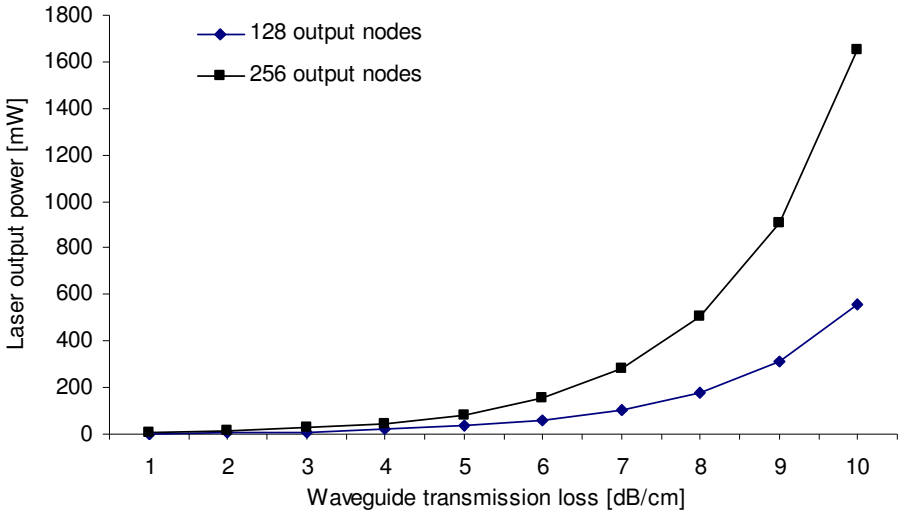


Fig.7.8. VCSEL optical output power required by the H-tree to provide a given BER vs. waveguide transmission loss.

Fig.7.9 and Fig.7.10 show the dependence of the optical power emitted by the VCSEL necessary to provide given system quality on the input and output coupling efficiency in 128 and 256 output nodes H-trees, respectively. Using currently available materials and methods it is theoretically possible to achieve an almost 50% input and 87% output coupling efficiency [SCH-98, SCH-00]. Although research progress in recent years has been substantial, the technology is not yet mature and from the figures it is evident that potential improvements in the technology can lead to a significant decrease in the total power dissipated in the optical system.

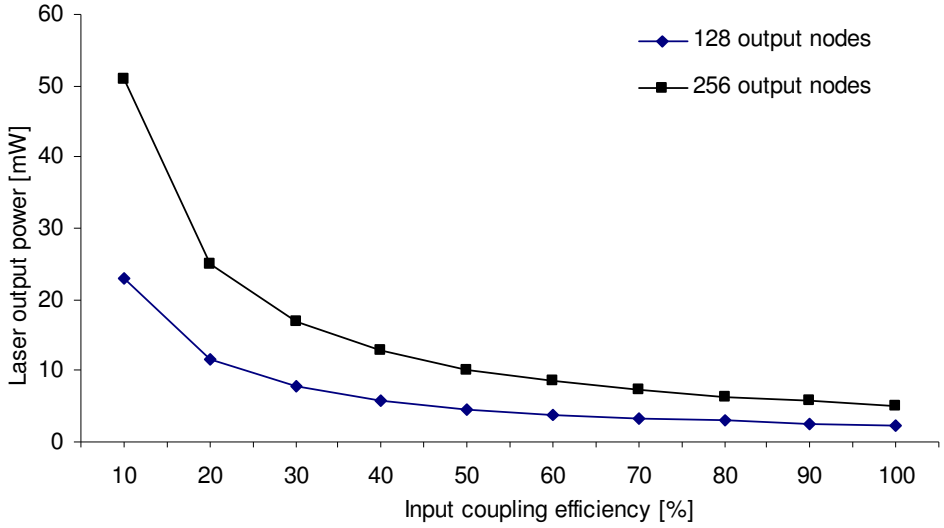


Fig.7.9 VCSEL optical output power required by the H-tree vs. input coupling efficiency.

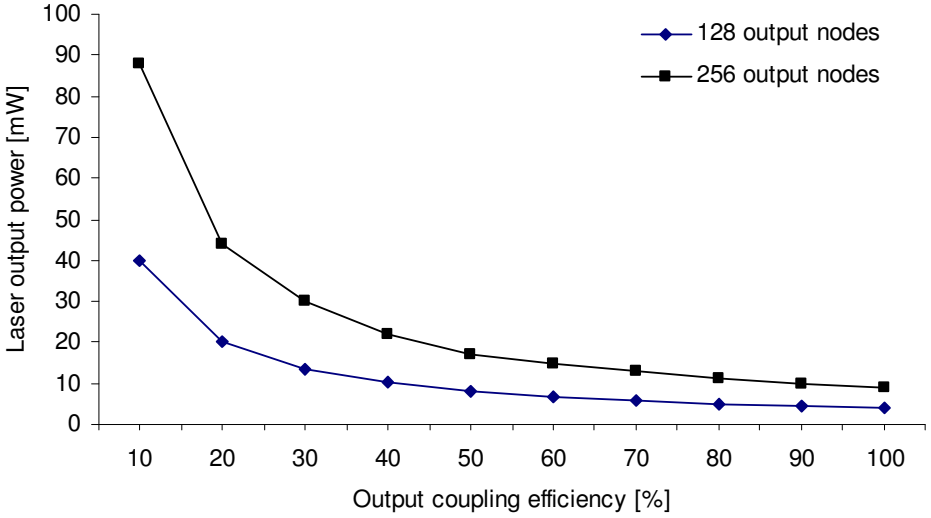


Fig.7.10. VCSEL optical output power required by the H-tree vs. output coupling efficiency.

Fig.7.11 presents the optical power emitted by the VCSEL for different values of losses introduced by Y-splitters. Due to the large number of Y-splitters in the optical clock system (255 in 256 output nodes H-tree) their contribution to total optical losses is

significant, even if the loss per Y-splitter is as small as 0.2dB. Decreasing the loss per Y-splitter from 0.5dB to 0.1dB leads to a 2 times smaller optical power emitted by the VCSEL.

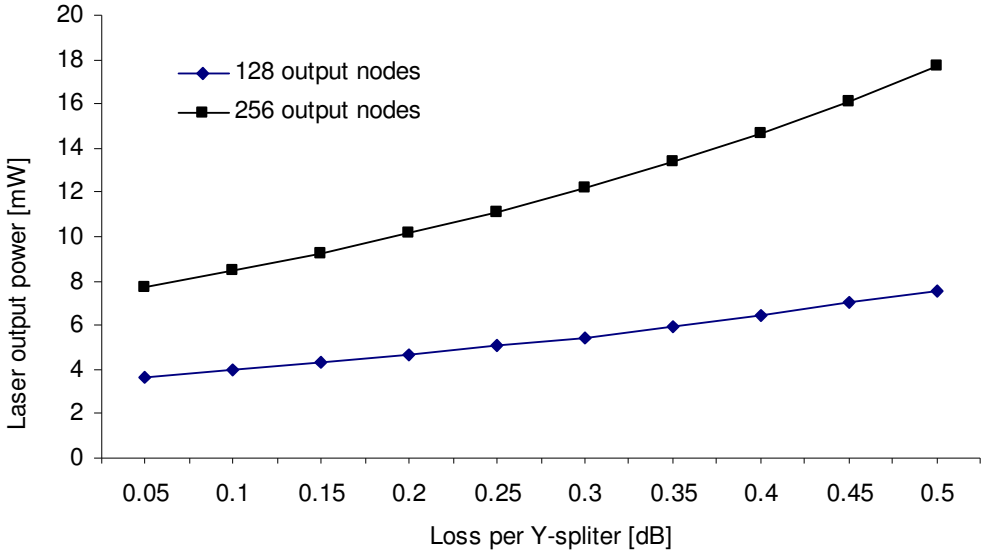
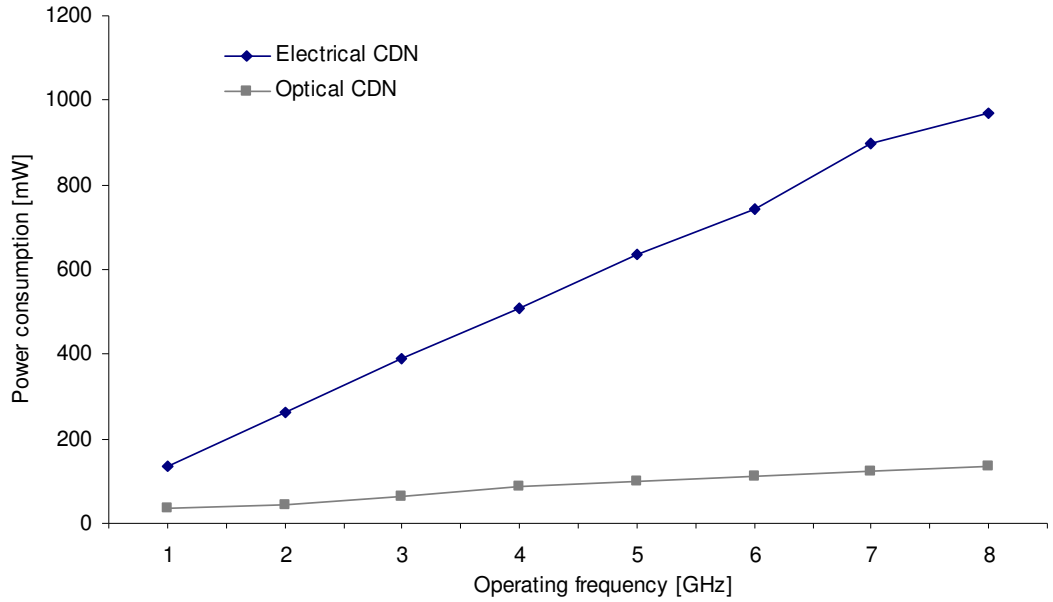


Fig.7.11. VCSEL optical output power required by the H-tree to provide a given BER vs. loss per Y-splitter.

7.4 COMPARISON OF OPTICAL AND ELECTRICAL SYSTEMS.

In order to carry out an unambiguous comparison in terms of dissipated power between the electrical and optical clock systems, the afore-presented realistic models for the H-tree CDN have been used. These models, built into the software packages ICAL and OPTO-ICAL, allow the calculation of the static and dynamic power consumptions of any components associated with both systems under different operating and design conditions. The results of simulations are collected in the figures covering their presentation in a comparative form that makes the evaluation of the effectiveness of replacing the global electrical clock tree by its optical counterpart easier. Since the number of output nodes in the global clock tree is usually limited to several dozen, in the majority of simulations, the considered global clock tree covered 128 or 256 output nodes, respectively.

a)



b)

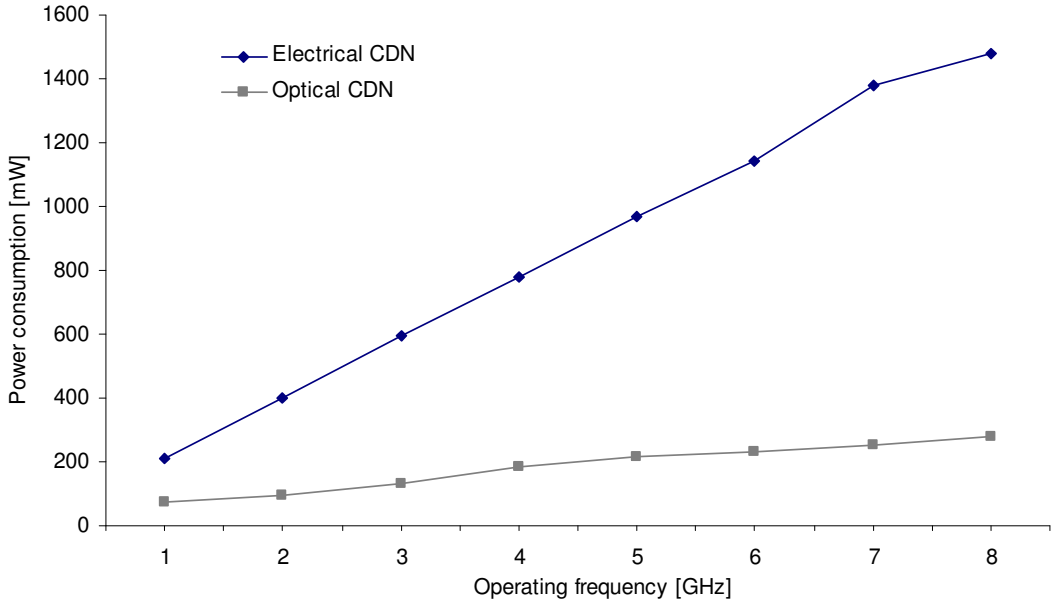
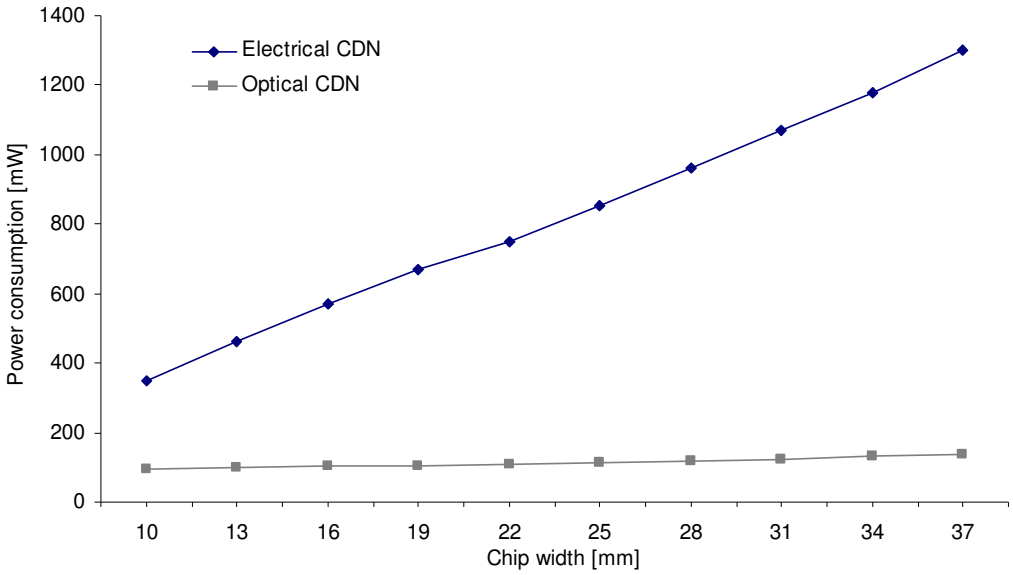


Fig.7.12. Electrical power consumption for optical and electrical CDN's versus different operating frequency. a) 128 output nodes b) 256 output nodes.

Fig.7.12 shows the variations of the power consumption for both electrical and optical clock systems as a function of operating frequency calculated for the receivers designed according to the 70nm technology node rules. The difference between both CDN solutions is easily noticed. Whereas the power consumption in the electrical system increases rapidly with the increase of the clock frequency, in the optical system the power consumption increases slowly and remains almost on the same level. At the 8GHz frequency, both in the 256 node H-tree and in the 128 node one, the power consumption in the optical system is more then 6 times smaller than in the electrical one.

In Fig.7.13 the power consumption for both electrical and optical clock systems is plotted as a function of chip width for a frequency equal to 5.6GHz and the receivers designed according to the 70nm technology node rules. In the case of electrical clock systems, the power consumption increases drastically along with the enlargement of die size. It is caused by the fact that both the length of the interconnects and the number of buffers increase, resulting in a bigger wiring and buffer capacitance, and consequently in the increase of dynamic power dissipation. In the case of the optical system, the power consumption remains almost on the same level. This can be explained by the fact that the optical waveguide losses due to the waveguide length contributes only to a small part of the total optical loss in the system. Thus the power consumed by the VCSEL increases insignificantly. Additionally, as it was shown in Fig.7.7. for the 256 nodes optical H-tree, receivers are the major power contributors in the optical system.

a)



b)

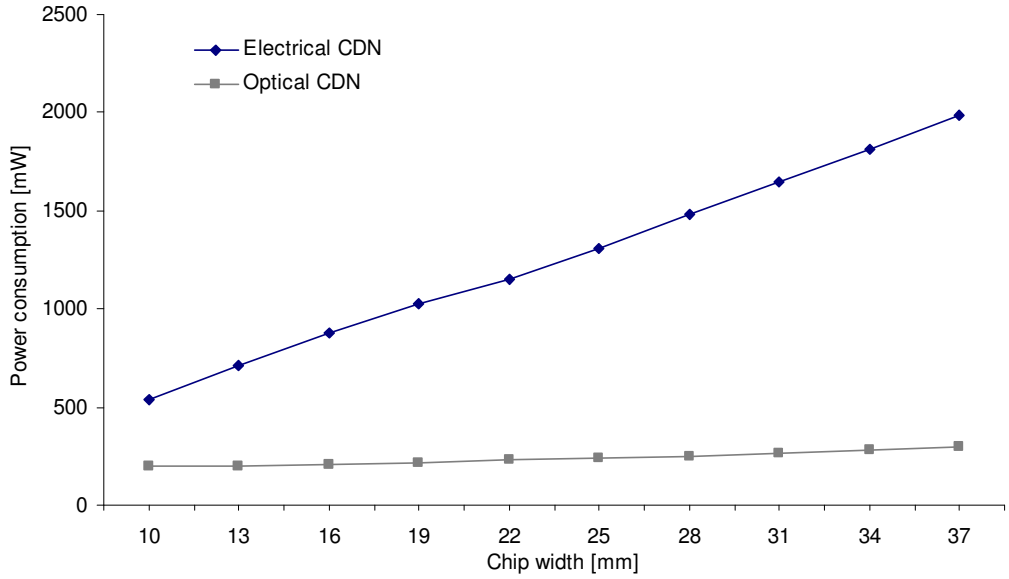
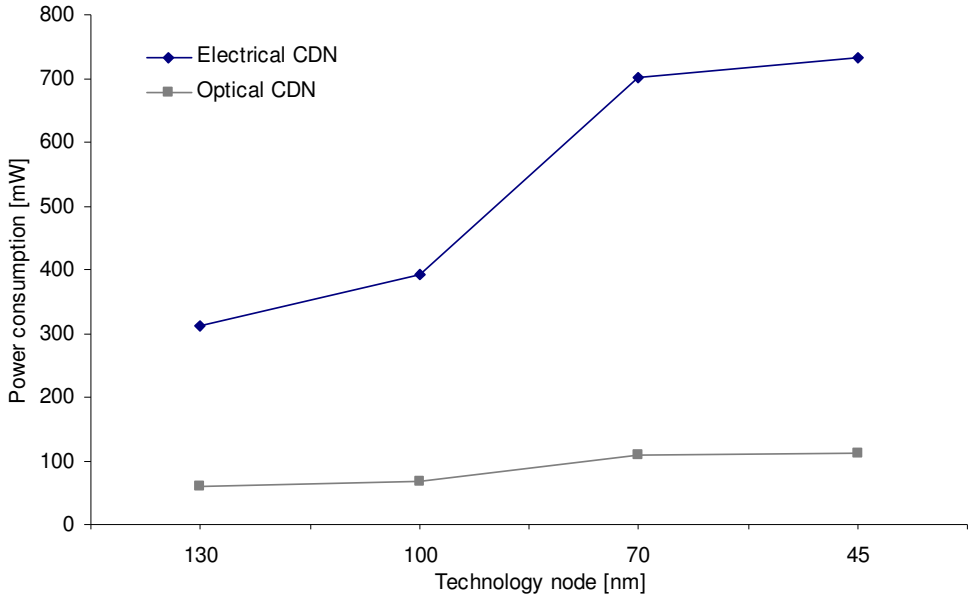


Fig.7.13. Electrical power consumption of optical and electrical CDN's versus different chip width. a) 128 output nodes b) 256 output nodes.

a)



b)

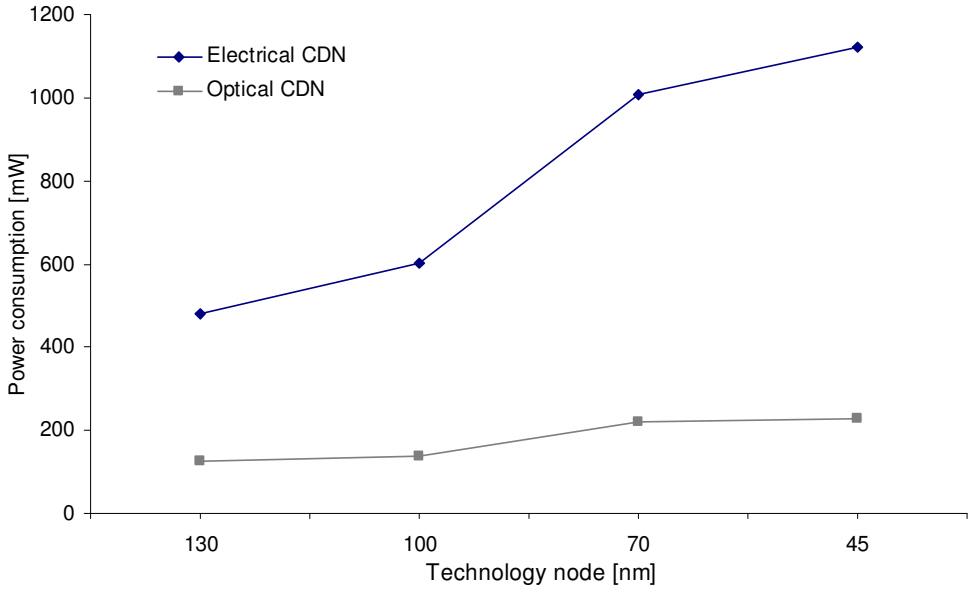


Fig.7.14. Electrical and optical power consumption versus various technology nodes. a) 128 output nodes b) 256 output nodes

The comparison between the electrical and optical clock distribution networks in terms of dissipated power as a function of different technology nodes is shown in Fig.7.14. One should note that in the case of electrical systems, all parameters used to calculate the power dissipation at each technology node are taken from ITRS predictions whereas the estimation of power consumption in the optical system based on the ITRS predictions in the case of the optical receivers only, and on the currently available optical technology in the case of optical devices. The presented results show that as the technology changes towards smaller technology nodes, the difference between power consumption in the electrical and optical clock distribution systems tends to increase to the optical system's advantage. At the 45nm technology node, the power consumed by the optical system is 5 times smaller than the electrical one and it is expected that when the optical technology is improved this difference should be even larger. This is especially true in the case of the laser wall-plug efficiency that is equal to the output light energy divided by the electrical energy into the wall plug, which is as low as 10-14 % in the considered VCSEL. Since VCSEL is the major contributor to overall optical system power consumption, the improving of its efficiency will increase the possible output power and reliability of these laser systems greatly.

Although the global clock distribution H-tree is usually limited to the 128-256 outputs nodes, it has been checked how the increase of the number of output nodes on a die with the constant width 20mm influences the system power consumption. The obtained results are collected in Fig.7.15. For a small number of H-tree nodes the power consumed by the optical H-tree is more than one order smaller than in the electrical one. However, along with the growth of circuit complexity, the advantages of the optical system tend to decrease. Finally, at the 8172 output nodes in considered case, the power consumed by optical system becomes larger than by electrical one. This fact can be easily explained taking into consideration the optical power budget summarized in Table 7.4. Along with doubling the number of H-tree output nodes, the optical power, which needs to be emitted by the VCSEL to meet overall system quality, increases at least by 3.2dB (because of the Y-splitters) what increases the electrical power consumed by VCSEL by more than 100%. Additionally, since the number of receivers is equal to the H-tree output nodes, the power consumed by receivers also doubles. In the case of electrical system, the power consumption increases significantly slower.

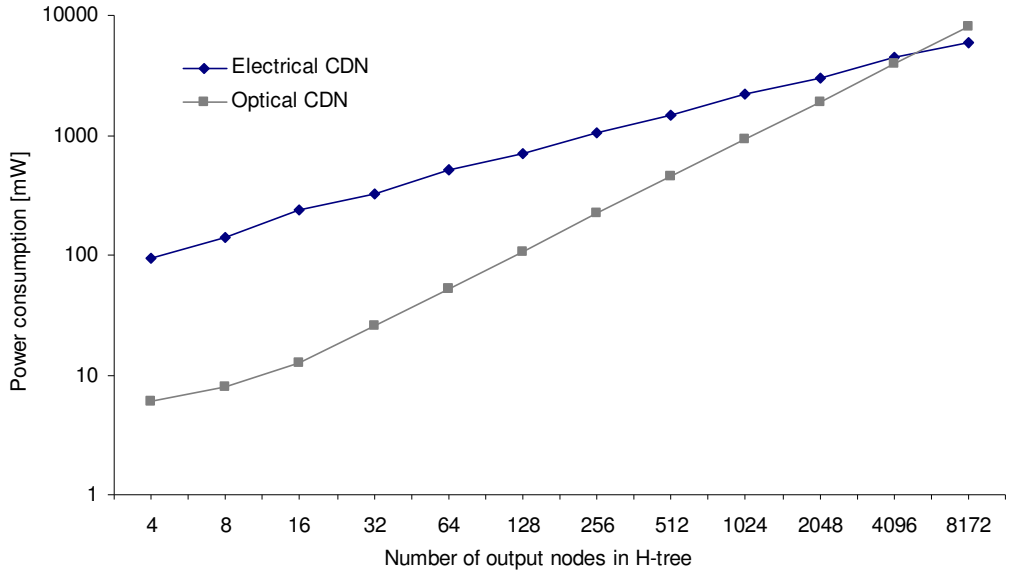


Fig.7.15. Electrical power consumption of optical and electrical CDN's versus various number of H-tree nodes (20mm chip width).

It is clear from Fig.7.15 that for a given chip size the amount of the power saved by an optical clock distribution network is significantly larger than for the small number of H-tree output nodes. In order to evaluate the effectiveness of the electrical global clock tree replacing by the optical system, the percentage amount of the saved power in considered chip size has been determined as a function of H-tree output nodes. The results are plotted in Fig.7.16. The black line represents the percentage amount of the saved power relative to the power consumed by the equivalent electrical tree, whereas the gray line represents the percentage amount of the saved power relative to the total power consumed by the 'boundary CDN system' defined as the H-tree at which the power consumption by the electrical clock becomes equal to the power consumption by the optical one. In the considered case, it is the 4096 output node H-tree with 4450mW power consumption.

As it is shown in Fig.7.16. the power dissipated in optical H-tree with 4 output nodes is almost 95% smaller than in equivalent electrical system, however replacing the 4 node electrical H-tree by 4 node optical H-tree leads to 2% power reduction only with reference to the power consumed by 'boundary CDN system'. On the other hand, replacing the electrical 1024 node H-tree by 1024 node optical H-tree in the 'boundary CDN system'

lead to almost 30% saving power, despite the fact that the power consumption by the optical clock system is only 2 times smaller than in the equivalent electrical tree.

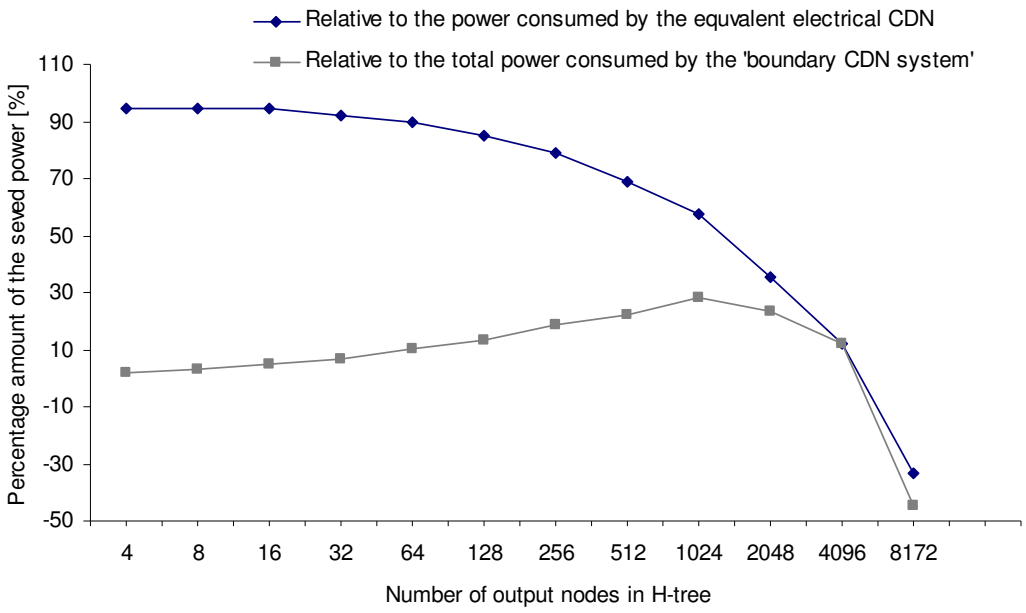
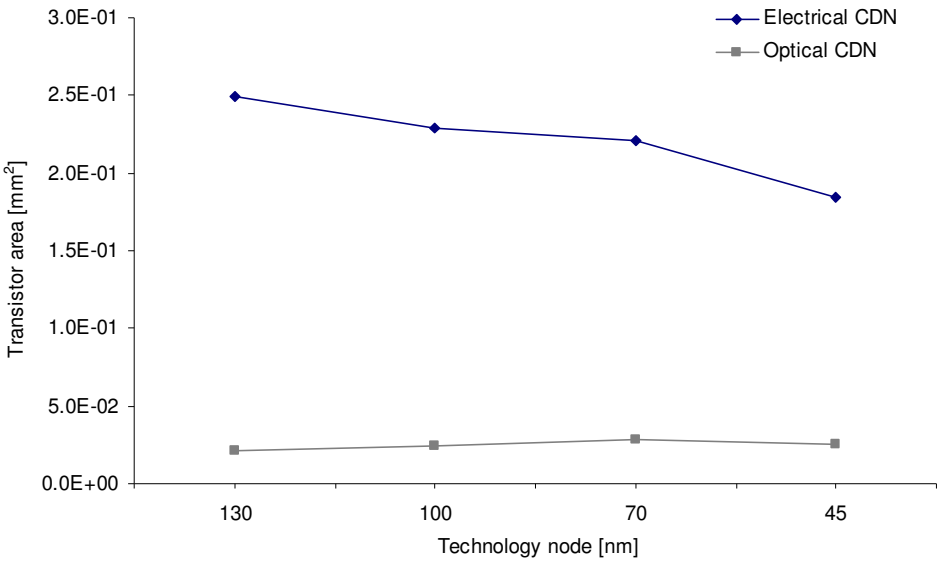


Fig.7.16. The percentage amount of the saved power versus various number of H-tree output nodes.

The total area occupied by the transistor is another important factor of the CDN design that has been compared for 128 and 256 H-tree nodes electrical and optical clock systems designed for different values of the technology node. The results of calculations are plotted as a function of the technology node in Fig.7.17. In the case of the electrical clock system, the area occupied by buffers decreases in spite of the increasingly large number of transistors. It is caused by higher integration density. In the case of an optical clock, the area increases insignificantly a cause of the assumed simply transimpedance circuit that can be not adequate for high frequency operation.

a)



b)

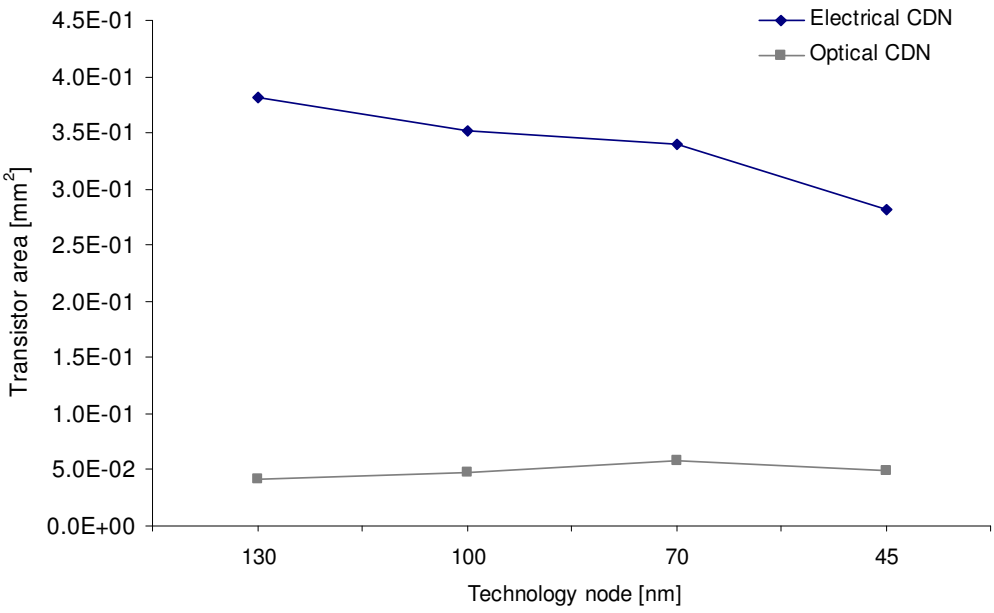


Fig.7.17. The total area occupied by electrical and optical clock system vs. technology node. a) 128 output nodes b) 256 output nodes.

7.5 CONCLUSION.

In this chapter the power consumption in both electrical and optical global H-tree clock distribution systems for future technology nodes have been calculated. In the case of electrical distribution, the power consumption takes into account the power dissipated in the buffers and by the interconnects of an optimized balanced H-tree. In the case of an optical clock distribution system, the calculations take into account the power dissipated in the optoelectronic conversion circuits; the power dissipated by the optical receivers and the energy needed by the optical source to provide the required optical output power. Electrical and optical systems have been compared in terms of dissipated power for the considered range of technology nodes. It was shown that in any considered case, the proposed optical clock network consumed significantly less energy than its electrical counterpart

VIII. Summary and Future Work

Chapter VIII

Summary and Future Work

8.1 SUMMARY OF THESIS.

This study has focused on the investigation of integrated optics as a possible alternative to overcome limitations due to metallic interconnections. It aims at the quantification of the reduction in power consumption both in present ICs and in these predicted by the ITRS roadmap, when an optical interconnect network replaces its electrical counterpart. Since the clock distribution network (CDN) is the most representative component of interconnections in modern VLSI circuits consuming a huge part of the delivered power, it has been chosen as the object of our numerical investigations. During the investigations, the H-tree architecture of CDN design (the most representative architecture for large clock distribution systems) was considered as the test network, realised in both optical and electrical domains, and the power consumption was used as the main comparison criterion.

The power consumption in the main balanced H-tree corresponding to classical electrical clock distribution systems for parameters of future technology generations predicted by the ITRS have been calculated. In this order, the distributed models of such an H-tree have been worked out and implemented in the software package ICAL, developed especially to analyse such a CDN system. It allows the determination an optimised balanced H-tree for considered input data and calculating its electrical parameters as well as power dissipation taking into account both the power dissipated in the buffers and in the interconnection wires. The power dissipated in the electrical system has been extracted from transistor-level simulations.

In order to ensure the equivalence between the electrical and optical solutions, the optical H-tree network has been designed identically as the global electrical H-tree

considered in the work. In the optical CDN system, a low-power VCSEL was used as an off-chip photonic source that was coupled into the H-tree symmetrical waveguide structure and provides the clock signal to *n* optical receivers. At the receivers, the high speed optical signal was converted to an electrical signal and subsequently distributed by the local electrical networks. In the case of the optical clock distribution system, the calculations took into account the power dissipated in the optoelectronic conversion circuits that were designed to meet the specified overall optical system performance and the losses of optical power in waveguide transmission lines. In order to do this properly, firstly power dissipated by the optical receivers was estimated then the energy needed by the optical source to provide the required optical output power.

The developed optical and electrical CDN models allowed the unambiguous comparison between the electrical and optical clock systems in terms of dissipated power. It was shown that the proposed optical clock network consumed significantly less energy than its electrical counterpart. Particularly, in the case of 45nm technology node, the power consumed by a 256 node optical H-tree system is over 5 times less than the power dissipated in the equivalent electrical system. One can expect that this ratio will be even larger with improved optical technology. Additionally, investigations performed for the 70nm technology node show that as the operating frequency and chip size increase the difference between the power consumption in both electrical and optical systems tends to grow.

One can conclude that the basic foundation of this thesis has been laid. It has been proved that the introduction of an optical clock distribution network, in place of the electric one will reduce the power consumption in essential way. The proposed optical solution allows the distribution of high local frequency signals across the chip with significantly smaller power dissipation than the electrical one.

8.2 FUTURE WORK.

Although in this work only the power consumption is compared one can expect lower crosstalk and clock skew in optical system. Thus, it is desirable to develop a proper timing models for both electrical and optical systems necessary to characterize clock skew and crosstalk associated with both system.

The next step of the project is to produce prototypes for the main elementary building blocks (III-V laser microsources, polycrystalline silicon microguides, laser-guide coupling) necessary to the fabrication of optical links capable of high-density integration onto VLSI circuits

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- G.Tosik, Z.Lisik, F.Gaffiot, I.O'Connor *Power Dissipation in Optical and Metallic Clock Distribution Networks in New VLSI Technologies* IEE Electronics Letters No.3 issue 5, Feb. 2004.
- F. Tissafi-Drissi, F. Mieyeville, I.O'Connor, G.Tosik, F.Gaffiot *Predictive Design Space Exploration of Maximum Bandwidth CMOS Photoreceiver Preamplifiers* ICECS 2003 December 14-17, 2003, United Arab Emirates.
- G.Tosik, F.Gaffiot, I.O'Connor, Z.Lisik F. Tissafi-Drissi *Optical versus Electrical Clock System in Future VLSI Technologies* 2003 International SOC Conference September 17-20,2003, Portland, Oregon, USA.
- G.Tosik, F.Gaffiot, I.O'Connor, Z.Lisik, F. Tissafi-Drissi *Optical versus Metallic Interconnections for Clock Distribution Networks in New VLSI* 'PATMOS 2003' September 10-12, 2003 Torino, Italy
- G.Tosik, Z.Lisik *Application Of Optical Solutions For The Clock Distribution In VLSI Circuits* 'MICROTHERM 2003' 29.06 - 2.07. 2003 Lodz, Poland
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Appendix A

BSIM models

From http://www-device.eecs.berkeley.edu/~ptm

```
*
* Predictive Technology Model Beta Version
* 0.13um NMOS SPICE Parametersv (normal one)
*

.model NMOS NMOS
+Level = 49

+Lint = 2.5e-08 Tox = 3.3e-09
+Vth0 = 0.332 Rdsw = 200

+lmin=1.3e-7 lmax=1.3e-7 wmin=1.3e-7 wmax=1.0e-4 Tref=27.0 version =3.1
+Xj= 4.5000000E-08          Nch= 5.6000000E+17
+lln= 1.0000000            lwn= 0.00                  wln= 0.00
+wwn= 1.0000000            ll= 0.00
+lw= 0.00                  lwl= 0.00                  wint= 0.00
+wl= 0.00                  ww= 0.00                   wwl= 0.00
+Mobmod= 1                 binunit= 2                 xl= 0
+xw= 0                     binflag=  0
+Dwg= 0.00                 Dwb= 0.00

+K1= 0.3661500              K2= 0.00
+K3= 0.00                  Dvt0= 8.7500000            Dvt1= 0.7000000
+Dvt2= 5.0000000E-02       Dvt0w= 0.00                Dvt1w= 0.00
+Dvt2w= 0.00               Nlx= 3.5500000E-07         W0= 0.00
+K3b= 0.00                 Ngate= 5.0000000E+20

+Vsat= 1.3500000E+05       Ua= -1.8000000E-09         Ub= 2.2000000E-18
+Uc= -2.9999999E-11        Prwb= 0.00
+Prwg= 0.00                Wr= 1.0000000              U0= 1.3400000E-02
+A0= 2.1199999             Keta= 4.0000000E-02        A1= 0.00
+A2= 0.9900000             Ags= -0.1000000            B0= 0.00
+B1= 0.00

+Voff= -7.9800000E-02      NFactor= 1.1000000         Cit= 0.00
+Cdsc= 0.00                Cdscb= 0.00                Cdscd= 0.00
+Eta0= 4.0000000E-02       Etab= 0.00                 Dsub= 0.5200000

+Pclm= 0.1000000           Pdiblc1= 1.2000000E-02     Pdiblc2= 7.5000000E-03
+Pdiblcb= -1.3500000E-02   Drout= 0.2800000          Pscbe1= 8.6600000E+08
+Pscbe2= 1.0000000E-20     Pvag= -0.2800000           Delta= 1.0100000E-02
+Alpha0= 0.00              Beta0= 30.0000000

+kt1= -0.3400000           kt2= -5.2700000E-02        At= 0.00
+Ute= -1.2300000           Ua1= -8.6300000E-10        Ub1= 2.0000001E-18
+Uc1= 0.00                 Kt1l= 4.0000000E-09        Prt= 0.00

+Cj= 0.0015                Mj= 0.7175511              Pb= 1.24859
```

```
+Cjsw= 2E-10               Mjsw= 0.3706993           Php= 0.7731149
+Cta= 9.290391E-04         Ctp= 7.456211E-04         Pta= 1.527748E-03
+Ptp= 1.56325E-03          JS=2.50E-08               JSW=4.00E-13
+N=1.0                     Xti=3.0                   Cgdo=2.75E-10
+Cgso=2.75E-10             Cgbo=0.0E+00              Capmod= 2
+NQSMOD= 0                 Elm= 5                    Xpart= 1
+Cgsl= 1.1155E-10          Cgdl= 1.1155E-10          Ckappa= 0.8912
+Cf= 1.113e-10             Clc= 5.475E-08            Cle= 6.46
+Dlc= 2E-08                Dwc= 0                    Vfbcv= -1

*
* Predictive Technology Model Beta Version
* 0.13um PMOS SPICE Parametersv (normal one)
*

.model PMOS PMOS
+Level = 49

+Lint = 2.e-08 Tox = 3.3e-09
+Vth0 = -0.3499 Rdsw = 400

+lmin=1.3e-7 lmax=1.3e-7 wmin=1.3e-7 wmax=1.0e-4 Tref=27.0 version =3.1
+Xj= 4.5000000E-08         Nch= 6.8500000E+18
+lln= 0.00                 lwn= 0.00                 wln= 0.00
+wwn= 0.00                 ll= 0.00
+lw= 0.00                  lwl= 0.00                 wint= 0.00
+wl= 0.00                  ww= 0.00                  wwl= 0.00
+Mobmod=  1                binunit= 2                xl=  0
+xw=  0                    binflag=  0
+Dwg= 0.00                 Dwb= 0.00
+K1= 0.4087000             K2= 0.00
+K3= 0.00                  Dvt0= 5.0000000           Dvt1= 0.2600000
+Dvt2= -1.0000000E-02      Dvt0w= 0.00               Dvt1w= 0.00
+Dvt2w= 0.00               Nlx= 1.6500000E-07        W0= 0.00
+K3b= 0.00                 Ngate= 5.0000000E+20

+Vsat= 1.0500000E+05       Ua= -1.4000000E-09        Ub= 1.9499999E-18
+Uc= -2.9999999E-11        Prwb= 0.00
+Prwg= 0.00                Wr= 1.0000000             U0= 5.2000000E-03
+A0= 2.1199999             Keta= 3.0300001E-02       A1= 0.00
+A2= 0.4000000             Ags= 0.1000000            B0= 0.00
+B1= 0.00

+Voff= -9.10000000E-02     NFactor= 0.1250000        Cit= 2.7999999E-03
+Cdsc= 0.00                Cdscb= 0.00               Cdscd= 0.00
+Eta0= 80.0000000          Etab= 0.00                Dsub= 1.8500000

+Pclm= 2.5000000           Pdiblc1= 4.8000000E-02    Pdiblc2= 5.0000000E-05
+Pdiblcb= 0.1432509        Drout= 9.0000000E-02      Pscbe1= 1.0000000E-20
+Pscbe2= 1.0000000E-20     Pvag= -6.0000000E-02      Delta= 1.0100000E-02
+Alpha0= 0.00              Beta0= 30.0000000

+kt1= -0.3400000           kt2= -5.2700000E-02       At= 0.00
+Ute= -1.2300000           Ua1= -8.6300000E-10       Ub1= 2.0000001E-18
+Uc1= 0.00                 Kt1l= 4.0000000E-09       Prt= 0.00

+Cj= 0.0015                Mj= 0.7175511             Pb= 1.24859
+Cjsw= 2E-10               Mjsw= 0.3706993           Php= 0.7731149
+Cta= 9.290391E-04         Ctp= 7.456211E-04         Pta= 1.527748E-03
+Ptp= 1.56325E-03          JS=2.50E-08              JSW=4.00E-13
+N=1.0                     Xti=3.0                  Cgdo=2.75E-10
+Cgso=2.75E-10             Cgbo=0.0E+00             Capmod= 2
+NQSMOD= 0                 Elm= 5                   Xpart= 1
+Cgsl= 1.1155E-10          Cgdl= 1.1155E-10         Ckappa= 0.8912
+Cf= 1.113e-10             Clc= 5.475E-08           Cle= 6.46
+Dlc= 2E-08                Dwc= 0                   Vfbcv= -1
```

```
*
* Predictive Technology Model Beta Version
* 0.10um NMOS SPICE Parametersv (normal one)
*

.model NMOS NMOS
+Level = 49

+Lint = 2.e-08 Tox = 2.5e-09
+Vth0 = 0.2607 Rdsw = 180

+lmin=1.0e-7 lmax=1.0e-7 wmin=1.0e-7 wmax=1.0e-4
+Tref=27.0   version =3.1
+Xj= 4.0000000E-08       Nch= 9.7000000E+17
+lln= 1.0000000          lwn= 1.0000000              wln= 0.00
+wwn= 0.00               ll= 0.00
+lw= 0.00                lwl= 0.00                   wint= 0.00
+wl= 0.00                ww= 0.00                    wwl= 0.00
+Mobmod=  1              binunit= 2                  xl= 0.00
+xw= 0.00                binflag=  0
+Dwg= 0.00               Dwb= 0.00

+ACM= 0                  ldif=0.00                   hdif=0.00
+rsh= 7                  rd= 0                       rs= 0
+rsc= 0                  rdc= 0

+K1= 0.3950000           K2= 1.0000000E-02           K3= 0.00
+Dvt0= 1.0000000         Dvt1= 0.4000000             Dvt2= 0.1500000
+Dvt0w= 0.00             Dvt1w= 0.00                 Dvt2w= 0.00
+Nlx= 4.8000000E-08      W0= 0.00                    K3b= 0.00
+Ngate= 5.0000000E+20

+Vsat= 1.1000000E+05     Ua= -6.0000000E-10          Ub= 8.0000000E-19
+Uc= -2.9999999E-11
+Prwb= 0.00              Prwg= 0.00                  Wr= 1.0000000
+U0= 1.7999999E-02       A0= 1.1000000               Keta= 4.0000000E-02
+A1= 0.00                A2= 1.0000000               Ags= -1.0000000E-02
+B0= 0.00                B1= 0.00

+Voff= -2.9999999E-02    NFactor= 1.5000000          Cit= 0.00
+Cdsc= 0.00              Cdscb= 0.00                 Cdscd= 0.00
+Eta0= 0.1500000         Etab= 0.00                  Dsub= 0.6000000

+Pclm= 0.1000000         Pdiblc1= 1.2000000E-02      Pdiblc2= 7.5000000E-03
+Pdiblcb= -1.3500000E-02 Drout= 2.0000000            Pscbe1= 8.6600000E+08
+Pscbe2= 1.0000000E-20   Pvag= -0.2800000           Delta= 1.0000000E-02
+Alpha0= 0.00            Beta0= 30.0000000

+kt1= -0.3700000         kt2= -4.0000000E-02         At= 5.5000000E+04
+Ute= -1.4800000         Ua1= 9.5829000E-10          Ub1= -3.3473000E-19
+Uc1= 0.00               Kt1l= 4.0000000E-09         Prt= 0.00

+Cj= 0.0015             Mj= 0.72                    Pb= 1.25
+Cjsw= 2E-10            Mjsw= 0.37                  Php= 0.773
+Cjgate= 2E-14           Cta= 0                      Ctp= 0
+Pta= 0                  Ptp= 0                      JS=1.50E-08
+JSW=2.50E-13            N=1.0                       Xti=3.0
+Cgdo=3.493E-10          Cgso=3.493E-10              Cgbo=0.0E+00
+Capmod= 2               NQSMOD= 0                   Elm= 5
+Xpart= 1                cgsl= 0.582E-10             cgdl= 0.582E-10
+ckappa= 0.28            cf= 1.177e-10               clc= 1.0000000E-07
+cle= 0.6000000          Dlc= 2E-08                  Dwc= 0
```

```
*
* Predictive Technology Model Beta Version
* 0.10um PMOS SPICE Parametersv (normal one)
*

.model PMOS PMOS
+Level = 49

+Lint = 2.e-08 Tox = 2.5e-09
+Vth0 = -0.303 Rdsw = 300

+lmin=1.0e-7 lmax=1.0e-7 wmin=1.0e-7 wmax=1.0e-4
+Tref=27.0   version =3.1
+Xj= 4.0000000E-08             Nch= 1.0400000E+18
+lln= 1.0000000               lwn= 0.00                      wln= 0.00
+wwn= 1.0000000               ll= 0.00                       lw= 0.00
+lwl= 0.00                    wint= 0.00                     wl= 0.00
+ww= 0.00                     wwl= 0.00                      Mobmod=  1
+binunit= 2                   xl= 0.00                       xw= 0.00
+binflag=  0                  Dwg= 0.00                      Dwb= 0.00

+ACM= 0                       ldif=0.00                      hdif=0.00
+rsh= 7                       rd= 0                          rs= 0
+rsc= 0                       rdc= 0

+K1= 0.3910000                K2= 1.0000000E-02              K3= 0.00
+Dvt0= 2.6700001              Dvt1= 0.5300000                Dvt2= 5.0000E-
02
+Dvt0w= 0.00                  Dvt1w= 0.00                    Dvt2w= 0.00
+Nlx= 7.5000000E-08           W0= 0.00                       K3b= 0.00
+Ngate= 5.0000000E+20

+Vsat= 1.0500000E+05          Ua= -5.0000000E-10             Ub= 1.5000000E-
18
+Uc= -2.9999999E-11
+Prwb= 0.00                   Prwg= 0.00                     Wr= 1.0000000
+U0= 5.5000000E-03            A0= 2.0000000                  Keta= 4.0000E-
02
+A1= 0.00                     A2= 0.9900000                  Ags= -0.1000000
+B0= 0.00                     B1= 0.00

+Voff= -7.0000000E-02         NFactor= 1.5000000             Cit= 0.00
+Cdsc= 0.00                   Cdscb= 0.00                    Cdscd= 0.00
+Eta0= 0.2500000              Etab= 0.00                     Dsub= 0.8000000

+Pclm= 0.1000000              Pdiblc1= 1.2000000E-02         Pdiblc2=
7.5000000E-03
+Pdiblcb= -1.3500000E-02      Drout= 0.9000000               Pscbe1=
8.6600000E+08
+Pscbe2= 1.0000000E-20        Pvag= -0.2800000               Delta=
1.0100000E-02
+Alpha0= 0.00                 Beta0= 30.0000000

+kt1= -0.3400000              kt2= -5.2700000E-02            At= 0.00
+Ute= -1.2300000              Ua1= -8.6300000E-10            Ub1= 2.000001E-
18
+Uc1= 0.00                    Kt1l= 4.0000000E-09            Prt= 0.00

+Cj= 0.0015                   Mj= 0.7175511                  Pb= 1.24859
+Cjsw= 2E-10                  Mjsw= 0.3706993                Php= 0.7731149
+Cjgate= 2E-14                Cta= 9.290391E-04              Ctp= 7.456211E-
04
+Pta= 1.527748E-03            Ptp= 1.56325E-03               JS=2.50E-08
+JSW=4.00E-13                 N=1.0                          Xti=3.0
+Cgdo=3.49E-10                Cgso=3.49E-10                  Cgbo=0.0E+00
```

```
+Capmod= 2                    NQSMOD= 0                      Elm= 5
+Xpart= 1                     cgsl= 0.582E-10                cgdl= 0.582E-10
+ckappa= 0.28                 cf= 1.177e-10                  clc= 5.47500E-
08
+cle= 6.4600000               Dlc= 2E-08                     Dwc= 0



*
* Predictive Technology Model Beta Version
* 0.07um NMOS SPICE Parametersv (normal one)
*

.model NMOS NMOS
+Level= 49

+lint=1.6e-8  Tox=1.6e-9
+Vth0=0.2   Rdsw=150

+lmin=7.0e-8         lmax=7.0e-8            wmin=0.07e-6            wmax=1.0e-4
+Tref=27.0           version =3.1           Xj= 2.9999999E-08       Nch=
1.20E+18
+lln= 1.0000000      lwn= 1.0000000         wln= 0.00               wwn= 0.00

+ll= 0.00            lw= 0.00         lwl= 0.00      wint= 0.00            wl=
0.00
+ww= 0.00            wwl= 0.00        Mobmod=1       binunit=2  xl= 0.00   xw=
0.00
+Lmlt= 1             Wmlt= 1          binflag=0      Dwg= 0.00            Dwb=
0.00

+ACM= 0     ldif=0.00       hdif=0.00      rsh= 6 rd= 0 rs= 0 rsc= 0  rdc= 0

+K1= 0.3700000          K2= 1.0000000E-02     K3= 0.00
+Dvt0= 1.3000000        Dvt1= 0.5000000       Dvt2= 2.9999999E-02       Dvt0w=
0.00
+Dvt1w= 0.00            Dvt2w= 0.00           Nlx= 7.0000000E-08        W0= 0.00
+K3b= 0.00              Ngate= 5.0000000E+20

+Vsat= 1.1500000E+05    Ua= 5.0000000E-10     Ub= 1.0000000E-18      Uc=-2.9999E-
11
+Prwb= 0.00             Prwg= 0.0             Wr= 1.0 U0= 2.5E-02    A0= 1.5
+Keta= 4.0000000E-02    A1= 0.00              A2= 1.00000            Ags= -1.0E-
02
+B0= 0.00               B1= 0.00

+Voff= -0.1500000       NFactor= 1.5000000     Cit= 0.00    Cdsc= 0.00  Cdscb=
0.00
+Cdscd= 1.0000000E-14   Eta0= 0.2000000        Etab= 0.00   Dsub= 1.0000000

+Pclm= 0.2500000         Pdiblc1= 1.2000000E-02              Pdiblc2= 7.5000000E-
03
+Pdiblcb= -1.3500000E-02 Drout= 1.5000000                    Pscbe1=
8.6600000E+08
+Pscbe2= 1.0000000E-20   Pvag= -0.2800000                    Delta= 1.0000000E-02
+Alpha0= 0.00            Beta0= 30.0000000

+kt1= -0.3700000         kt2= -4.0000000E-02                 At= 5.5000000E+04
+Ute= -1.4800000         Ua1= 9.5829000E-10                  Ub1= -3.3473000E-19
+Uc1= 0.00               Kt1l= 4.0000000E-09                 Prt= 0.00

+Cj= 0.0015            Mj= 0.72           Pb= 1.25     Cjsw= 2E-10       Mjsw=
0.37
+Php= 0.773            Cjgate= 2E-14      Cta= 0 Ctp= 0 Pta= 0         Ptp= 0
+JS=1.50E-08           JSW=2.50E-13       N=1.0          Xti=3.0
```

```
+Cgdo=4.094E-10        Cgso=4.094E-10     Cgbo=0.0E+00               Capmod= 2
+NQSMOD= 0             Elm= 5 Xpart= 1    cgsl= 1.0010000E-10        cgdl=1.001E-
10
+ckappa= 0.08          cf= 1.28e-10       clc= 1.0000000E-07         cle= 0.60
+Dlc= 1.6E-08          Dwc= 0


*
* Predictive Technology Model Beta Version
* 0.07um PMOS SPICE Parametersv (normal one)
*

.model PMOS PMOS
+Level= 49

+Lint = 1.5e-08 Tox = 1.7e-09
+Vth0 = -0.22 Rdsw = 280

+lmin=7.0e-8           lmax=7.0e-8            wmin=0.07e-6             wmax=1.0e-
4
+Tref=27.0             version =3.1           Xj= 2.9999999E-08        Nch=
1.2E+18
+lln= 1.0000000        lwn= 0.00              wln= 0.00                wwn= 1.0

+ll= 0.00    lw= 0.00     lwl= 0.00              wint= 0.00    wl= 0.00    ww=
0.00
+wwl= 0.00   Mobmod=  1   binunit= 2             xl= 0.00      xw= 0.00
+Lmlt=  1    Wmlt=  1     binflag=  0            Dwg= 0.00     Dwb= 0.00

+ACM= 0     ldif=0.00    hdif=0.00    rsh= 7    rd= 0   rs= 0   rsc= 0    rdc= 0

+K1= 0.3800000         K2= 1.0000000E-02       K3= 0.00         Dvt0= 2.2000000
+Dvt1= 0.6500000       Dvt2= 5.0000000E-02     Dvt0w= 0.00      Dvt1w= 0.00

+Dvt2w= 0.00           Nlx= 8.0000000E-08 W0= 0.00 K3b= 0.00 Ngate= 5.0000000E+20

+Vsat= 8.5000000E+04       Ua= 1.8000000E-09           Ub= 3.0000000E-18
+Uc= -2.9999999E-11        Prwb= 0.00                  Prwg= 0.00          Wr=
1.00
+U0= 1.4500000E-02       A0= 1.2000000         Keta= 4.0000000E-02
+A1= 0.00                A2= 0.9900000         Ags= -0.1000000 B0= 0.00  B1= 0.00

+Voff= -0.1500000       NFactor= 1.2000000     Cit= 0.00                Cdsc=
0.00
+Cdscb= 0.00            Cdscd= 0.00            Eta0= 0.27  Etab= 0.00    Dsub=
0.95

+Pclm= 0.5500000         Pdiblc1= 1.2000000E-02      Pdiblc2= 7.5000000E-03
+Pdiblcb= -1.3500E-02    Drout= 0.9000000            Pscbe1= 8.6600000E+08
+Pscbe2= 1.0000000E-20   Pvag= -0.2800000           Delta= 1.0100000E-02
+Alpha0= 0.00            Beta0= 30.0000000

+kt1= -0.3400000         kt2= -5.2700000E-02 A        t= 0.00       Ute= -
1.2300000
+Ua1= -8.6300000E-10     Ub1= 2.0000001E-18          Uc1= 0.00
+Kt1l= 4.0000000E-09     Prt= 0.00

+Cj= 0.0015        Mj= 0.7175511     Pb= 1.24859       Cjsw= 2E-10
Mjsw=0.3706993
+Php= 0.7731149    Cjgate= 2E-14     Cta= 9.290391E-04 Ctp= 7.456211E-04
+Pta= 1.527748E-03 Ptp= 1.56325E-03  JS=2.50E-08       JSW=4.00E-13
+N=1.0             Xti=3.0           Cgdo=3.853E-10    Cgso=3.853E-10
Cgbo=0.0E+00
+Capmod= 2         NQSMOD= 0         Elm= 5            Xpart= 1    cgsl= 0.6422E-
10
+cgdl= 0.6422E-10  ckappa= 0.08      cf= 1.266e-10
```

```
+clc= 5.475E-08    cle= 6.4600000   Dlc= 1.5E-08
+Dwc= 0            Vfbcv= -1


*
* Predictive Technology Model Beta Version
* BPTM 45nm NMOS
*

.model  nmos  nmos  level = 54

+version = 4.0          binunit = 1           paramchk= 1          mobmod  = 0
+capmod  = 2            igcmod  = 1           igbmod  = 1          geomod  = 1
+diomod  = 1            rdsmod  = 0           rbodymod= 1          rgatemod= 1
+permod  = 1            acnqsmod= 0           trnqsmod= 0

+tnom    = 27           toxe    = 1.4e-009    toxp    = 7e-010  toxm    = 1.4e-
009
+dtox    = 0            epsrox  = 3.9         wint    = 5e-009  lint    = 1.2e-
008
+ll      = 0            wl      = 0           lln     = 1       wln     = 1
+lw      = 0            ww      = 0           lwn     = 1       wwn     = 1
+lwl     = 0            wwl     = 0           xpart   = 0       toxref  = 1.4e-
009

+vth0    = 0.22         k1      = 0.35        k2      = 0.05    k3      = 0
+k3b     = 0            w0      = 2.5e-006    dvt0    = 2.8     dvt1    = 0.52
+dvt2    = -0.032       dvt0w   = 0           dvt1w   = 0       dvt2w   = 0
+dsub    = 2            minv    = 0.05        voffl   = 0       dvtp0   = 1e-007
+dvtp1   = 0.05         lpe0    = 5.75e-008   lpeb    = 2.3e-010  xj      = 2e-
008
+ngate   = 5e+020       ndep    = 2.8e+018    nsd     = 1e+020       phin= 0
+cdsc    = 0.0002       cdscb   = 0           cdscd   = 0            cit = 0
+voff    = -0.15        nfactor = 1.2         eta0    = 0.15         etab = 0
+vfb     = -0.55        u0      = 0.032       ua      = 1.6e-010   ub = 1.1e-017
+uc      = -3e-011      vsat    = 1.1e+005    a0      = 2            ags= 1e-020
+a1      = 0            a2      = 1           b0      = -1e-020      b1   = 0
+keta    = 0.04         dwg     = 0           dwb     = 0            pclm  =
0.18
+pdiblc1 = 0.028        pdiblc2 = 0.022       pdiblcb = -0.005       drout =
0.45
+pvag    = 1e-020       delta   = 0.01        pscbe1  = 8.14e+008    pscbe2=1e-
007
+fprout  = 0.2          pdits   = 0.2         pditsd  = 0.23
pditsl=2.3e+6
+rsh     = 3            rdsw    = 150         rsw     = 150          rdw  = 150
+rdswmin = 0            rdwmin  = 0           rswmin  = 0            prwg = 0
+prwb    = 6.8e-011     wr      = 1           alpha0  = 0.074
alpha1=0.005
+beta0   = 30           agidl   = 0.0002      bgidl   = 2.1e+009
cgidl=0.0002
+egidl   = 0.8

+aigbacc = 0.012        bigbacc = 0.0028      cigbacc = 0.002
+nigbacc = 1            aigbinv = 0.014       bigbinv = 0.004
cigbinv=0.004
+eigbinv = 1.1          nigbinv = 3           aigc    = 0.012        bigc=
0.0028
+cigc    = 0.002        aigsd   = 0.012       bigsd   = 0.0028       cigsd=0.002
+nigc    = 1            poxedge = 1           pigcd   = 1            ntox= 1

+xrcrg1  = 12           xrcrg2  = 5
+cgso    = 6.238e-010   cgdo    = 6.238e-010  cgbo    = 2.56e-011   cgdl=2.495e-
10
+cgsl    = 2.495e-10    ckappas = 0.01        ckappad = 0.01         acde= 1
+moin    = 15           noff    = 0.9         voffcv  = 0.02
```

```
+kt1     = -0.37        kt1l    = 0.0           kt2     = -0.042        ute= -1.5
+ua1     = 1e-009    ub1     = -3.5e-019    uc1     = 0    prt     = 0
+at      = 53000

+fnoimod = 1            tnoimod = 0

+jss     = 0.0001       jsws    = 1e-011       jswgs   = 1e-010       njs     = 1
+ijthsfwd= 0.01         ijthsrev= 0.001        bvs     = 10           xjbvs   = 1
+jsd     = 0.0001       jswd    = 1e-011       jswgd   = 1e-010       njd     = 1
+ijthdfwd= 0.01         ijthdrev= 0.001        bvd     = 10           xjbvd   = 1
+pbs     = 1            cjs     = 0.0005       mjs     = 0.5          pbsws   = 1
+cjsws   = 5e-010       mjsws   = 0.33         pbswgs  = 1            cjswgs=3e-
010
+mjswgs  = 0.33         pbd     = 1            cjd     = 0.0005       mjd   = 0.5
+pbswd   = 1            cjswd   = 5e-010       mjswd   = 0.33         pbswgd  = 1
+cjswgd  = 5e-010       mjswgd  = 0.33         tpb     = 0.005        tcj
=0.001
+tpbsw   = 0.005        tcjsw   = 0.001        tpbswg  = 0.005
tcjswg=0.001
+xtis    = 3            xtid    = 3

+dmcg    = 0e-006       dmci    = 0e-006       dmdg    = 0e-006       dmcgt=0e-
007
+dwj     = 0.0e-008     xgw     = 0e-007       xgl     = 0e-008

+rshg    = 0.4          gbmin   = 1e-010       rbpb    = 5            rbpd    =
15
+rbps    = 15           rbdb    = 15           rbsb    = 15           ngcon   = 1


*
* Predictive Technology Model Beta Version
* BPTM 45nm PMOS
*

.model  pmos  pmos  level = 54

+version = 4.0          binunit = 1            paramchk= 1            mobmod  = 0
+capmod  = 2            igcmod  = 1            igbmod  = 1            geomod  = 1
+diomod  = 1            rdsmod  = 0            rbodymod= 1            rgatemod= 1
+permod  = 1            acnqsmod= 0            trnqsmod= 0

+tnom    = 27           toxe    = 1.4e-009     toxp    = 7e-010       tox=1.4e-
009
+dtox    = 0            epsrox  = 3.9          wint    = 5e-009       lint=1.2e-
008
+ll      = 0            wl      = 0            lln     = 1            wln     = 1
+lw      = 0            ww      = 0            lwn     = 1            wwn     = 1
+lwl     = 0            wwl     = 0            xpart   = 0          toxref=1.4e-
009

+vth0    = -0.22        k1      = 0.39         k2      = 0.05         k3      = 0
+k3b     = 0            w0      = 2.5e-006     dvt0    = 3.9          dvt1= 0.635
+dvt2    = -0.032       dvt0w   = 0            dvt1w   = 0            dvt2w   = 0
+dsub    = 0.7          minv    = 0.05         voffl   = 0           dvtp0=0.5e-
008
+dvtp1   = 0.05         lpe0    = 5.75e-008    lpeb    = 2.3e-010     xj   =2e-
008
+ngate   = 5e+020       ndep    = 2.8e+018     nsd     = 1e+020       phin    = 0
+cdsc    = 0.000258     cdscb   = 0            cdscd   = 6.1e-008     cit     = 0
+voff    = -0.15        nfactor = 2            eta0    = 0.15         etab    = 0
+vfb     = 0.55         u0      = 0.0095       ua      = 1.6e-009     ub   = 8e-
018
+uc      = 4.6e-013     vsat    = 90000        a0      = 1.2          ags  = 1e-
020
```

```
+a1      = 0           a2      = 1           b0      = -1e-020      b1      = 0
+keta    = -0.047      dwg     = 0           dwb     = 0            pclm = 0.55
+pdiblc1 = 0.03        pdiblc2 = 0.0055      pdiblcb = 3.4e-008     drout =
0.56
+pvag    = 1e-020      delta   = 0.014       pscbe1  = 8.14e+008 pscbe2=9.58e-
007
+fprout  = 0.2         pdits   = 0.2         pditsd  = 0.23
pditsl=2.3e+006
+rsh     = 3           rdsw    = 250         rsw     = 160          rdw     =
160
+rdswmin = 0           rdwmin  = 0           rswmin  = 0           prwg=3.22e-
008
+prwb    = 6.8e-011    wr      = 1           alpha0  = 0.074        alpha1=
0.005
+beta0   = 30          agidl   = 0.0002      bgidl   = 2.1e+009
cgidl=0.0002
+egidl   = 0.8

+aigbacc = 0.012       bigbacc = 0.0028      cigbacc = 0.002
+nigbacc = 1           aigbinv = 0.014       bigbinv = 0.004
cigbinv=0.004
+eigbinv = 1.1         nigbinv = 3           aigc    = 0.69         bigc=0.0012
+cigc    = 0.0008      aigsd   = 0.0087      bigsd   = 0.0012       cigsd=
0.0008
+nigc    = 1           poxedge = 1           pigcd   = 1            ntox= 1

+xrcrg1  = 12          xrcrg2  = 5
+cgso    = 7.43e-010   cgdo    = 7.43e-010   cgbo    = 2.56e-011    cgdl= 1e-
014
+cgsl    = 1e-014      ckappas = 0.5         ckappad = 0.5          acde    = 1
+moin    = 15          noff    = 0.9         voffcv  = 0.02

+kt1     = -0.34       kt11    = 0           kt2     = -0.052        ute = -1.5
+ua1     = -1e-009    ub1     = 2e-018    uc1     = 0    prt     = 0
+at      = 33000

+fnoimod = 1           tnoimod = 0

+jss     = 0.0001      jsws    = 1e-011      jswgs   = 1e-010       njs     = 1
+ijthsfwd= 0.01        ijthsrev= 0.001       bvs     = 10           xjbvs   = 1
+jsd     = 0.0001      jswd    = 1e-011      jswgd   = 1e-010       njd     = 1
+ijthdfwd= 0.01        ijthdrev= 0.001       bvd     = 10           xjbvd   = 1
+pbs     = 1           cjs     = 0.0005      mjs     = 0.5          pbsws   = 1
+cjsws   = 5e-010      mjsws   = 0.33        pbswgs  = 1            cjswgs=3e-
010
+mjswgs  = 0.33        pbd     = 1           cjd     = 0.0005       mjd     =
0.5
+pbswd   = 1           cjswd   = 5e-010      mjswd   = 0.33         pbswgd  = 1
+cjswgd  = 5e-010      mjswgd  = 0.33        tpb     = 0.005        tcj = 0.001
+tpbsw   = 0.005       tcjsw   = 0.001       tpbswg  = 0.005        tcjswg=
0.001
+xtis    = 3           xtid    = 3

+dmcg    = 5e-006      dmci    = 5e-006      dmdg    = 5e-006       dmcgt= 6e-
007
+dwj     = 4.5e-008    xgw     = 3e-007      xgl     = 4e-008

+rshg    = 0.4         gbmin   = 1e-010      rbpb    = 5            rbpd    =
15
+rbps    = 15          rbdb    = 15          rbsb    = 15           ngcon   = 1
```

Abstract

The purpose of this thesis is to provide an unambiguous comparison in terms of dissipated power between optical and electrical clock distribution networks (CDN). A study of on-chip metal interconnect performance as CMOS device technology scales down to nanometric dimensions has been done. Whereas transistor scaling provides improvements in both density and device performance, interconnect scaling improves interconnect density but generally at the cost of degraded propagation delay and power consumption. In a modern VLSI circuit with power dissipation of 100W, the clock tree uses at least 30% of this power and may even reach 50%. Due to natural limits in thermal management, this is a real barrier to further progress. This motivates the use of optical interconnects as an alternative solution that could overcome the limitations of metallic interconnects. Clock distribution networks could particularly benefit from this technology. A new optical H-tree clock distribution architecture, in which optical waveguides are used as the signal paths are proposed. For this structure, detailed comparative simulations in terms of power dissipation of both optical and electrical H-tree clock networks for future technology generation parameters have been performed. In the case of electrical clock distribution, the power consumption takes into account the power dissipated in the buffers and in the wires of an optimized balanced H-tree. In the case of optical CDN, the calculations take into account the power dissipated in the optoelectronic interface circuits (photoreceiver and transmitter). It is shown that the power consumption in optical H-tree is several times smaller then in the equivalent electrical clock network. The proposed solution of the optical H-tree allows the distribution of high local frequency signals across the chip, with significantly lower power dissipation than the electrical system.