SIEMENS

TELEPERM M

AS 235 H Automation System

Description C79000-T8076-C484-04

SIEMENS

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Contents

Appendix

Preface

This description deals with the system software and method of operation of the fault–tolerant AS 235 H automation system.

Method of operation, configuration, bus communication, function block processing, etc. of the AS 235 standard automation system are discussed in the Description “AS 235 Variant G” (Order No. C79000-T8076-C416).

The hardware configuration is described in the AS 235 H System Manual (Order No. C79000-G8076-C293).

Abbreviations

I, II	Identification numbers (Roman numerals) of the redundant subsystems (redundancies) within a multi–redundant system.
AA	Analog output module
AE	Analog input module
AF	Remote bus connector board
AS	Automation system
AZR	Flag register of the CPU 235
B	Backup (CPU status = synchronization and updating)
BA	Binary output module
B&B	Operator control and monitoring
BE	Binary input module
BGF	Module fault
BGNR	Module number
BGT	Subrack
BKA	Operator input channel interface module
BKU	Operator input channel switchover (video relay and adapter cable)
BL	Blinking clock–pulse generator module
CPU 235 H	Central processing unit 235 H
CS275	LAN for linking TELEPERM M systems (coupling systems)
DG	Diagnostic unit
DGA	Diagnostic unit interface module
DMA	Direct memory access
E/A	Input and output (I/O)
EABA	I/O bus interface module
EANK	One–out–of–n code; TELEPERM M procedure for detecting I/O addresses with no or multiple assignments
EAVU	I/O comparator and switchover module
EE	Extension unit
ES	Extension cabinet
EPROM	Ultraviolet erasable programmable read–only memory
F	Fail–safe (by redundancy) or mode: failure
FDC	Floppy–disk controller
FIFO	First in first out (queuing or handling hierarchy)
FTSP	Error when testing the coil voltage
GE	Basic unit
GS	Basic cabinet
H	Fault–tolerant (by redundancy)
HF	H and F in compatible combination
KF	Channel fault
L+	Positive supply voltage, 24 V rated value
LAN	Local area network; mid–range communications bus
LED	Light emitting diode
LOES	Clearing the user memory by entering the keyboard command ”LOES;”
LTM	I&C alarm

M	Master (CPU mode)
M	Earth, negative pole
MDA	Mini floppy disk interface module
MDE	Mini floppy disk unit
MDT	Mean downtime (mean time between the occurrence of a failure and operation restart)
ML	Alarm logic module
MTBF	Mean time between failures (mean time between two failure occurrences, i.e. faultless interval)
MZ	Off–load earth, reference potential for analog inputs
N–AS	Local bus interface module for automation systems
NAU	Power failure
N8	TELEPERM M local bus interface, 8 bits on CS 275 bus system
N8–H	N8 in a fault tolerant 1–out–of–2 master/reserve configuration of a redundant automation system
NV	Local bus distributor
OS	Operator control and monitoring system
P	Passive (asynchronous CPU status; no N8–H accesses etc.)
PBE	Testable binary input module
PBT	Process communication keyboard (TELEPERM M AS accessory)
PE	Protective earth, cabinet potential
PESP	Peripheral memory area
PM	L+ for alarm purposes
PRA	Testable relay output module
PROM	Programmable read–only memory
PS	L+ for logic “1” with 24-V inputs
PÜ	L+ for monitoring purposes
PU	Process interrupt
PU5	Standard: unassigned process interrupt No. 5 (PU5) which is exclusively used for redundancy–related purposes
PUM	Buffer module
QVZ	Time–out during memory or peripheral access
R	Standby (CPU mode)
RAM	Random access memory
RDY	Ready
ROM	Read–only memory
RSOF	Software reset
SAE	Cabinet connection element
SB	Synchronization module
SED	Cabinet power supply diode
SEP	Standard plug–in station in a subrack, 15.24 mm wide
SES	Cabinet power supply unit
SF	Signal interface module
SF61	Signal interface module in slot address 61 (mnemonic name for a group interrupt module in this slot; 48–binary input module)
SP	Memory module
STA	Starting block processing
STO	Halting block processing
SV	Power supply module
SVE	Power supply unit
SVME	Power supply unit for extension unit
SW	Software

TM	TELEPERM M
UI	Inductive bus converter unit for CS275
VD 11	Logic diode module for messages
VKB	Comparator coupler module
VR	Video relay
ZE	Central processing unit
ZEP	Central earthing point
ZRS	Central reset
ZT	Central unit (subrack containing CPU I and CPU II)

 C79000–T8076–C484–04

1 System Summary

1.1 Basic Structure of the AS 235 H System

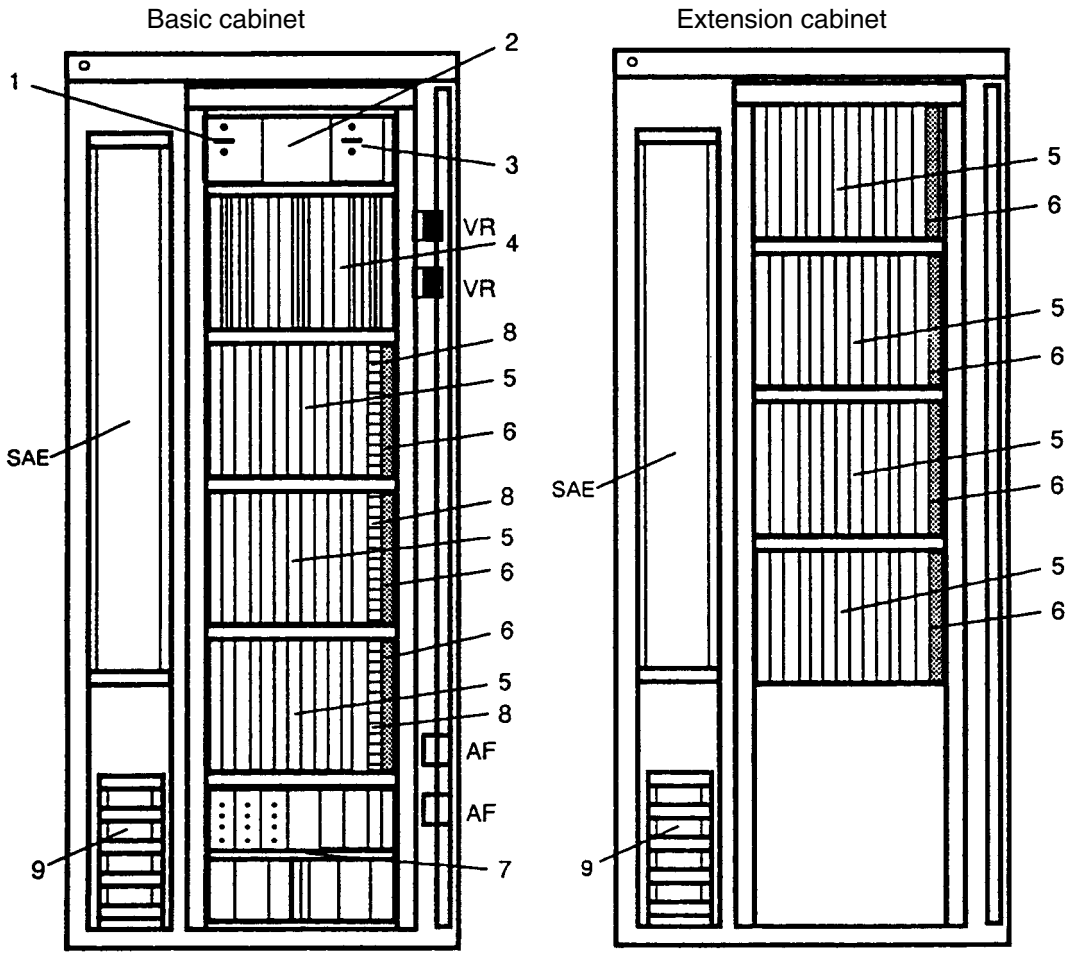
The AS 235 H automation system is the fault–tolerant version of the AS 235 automation system. Fault–tolerance is achieved by redundant [1)] use of two central processing units. The second CPU continues operation if the first unit fails. Redundancy can only be maintained if **all** resources are monitored, serviced and repaired.

This description only contains a general layout plan of the AS 235 H system (see Fig. 1.1). Please refer to the AS 235 H Manual (Section 1) for detailed hardware descriptions.

Fig. 1.2 shows the redundant structure of the AS 235 H system. The central unit consists of two central processing units with synchronous clock and command execution which operate as a 1–out–of–2 system. The second, faultless CPU of a redundant system continues process execution if the master CPU fails or contains a hardware fault.

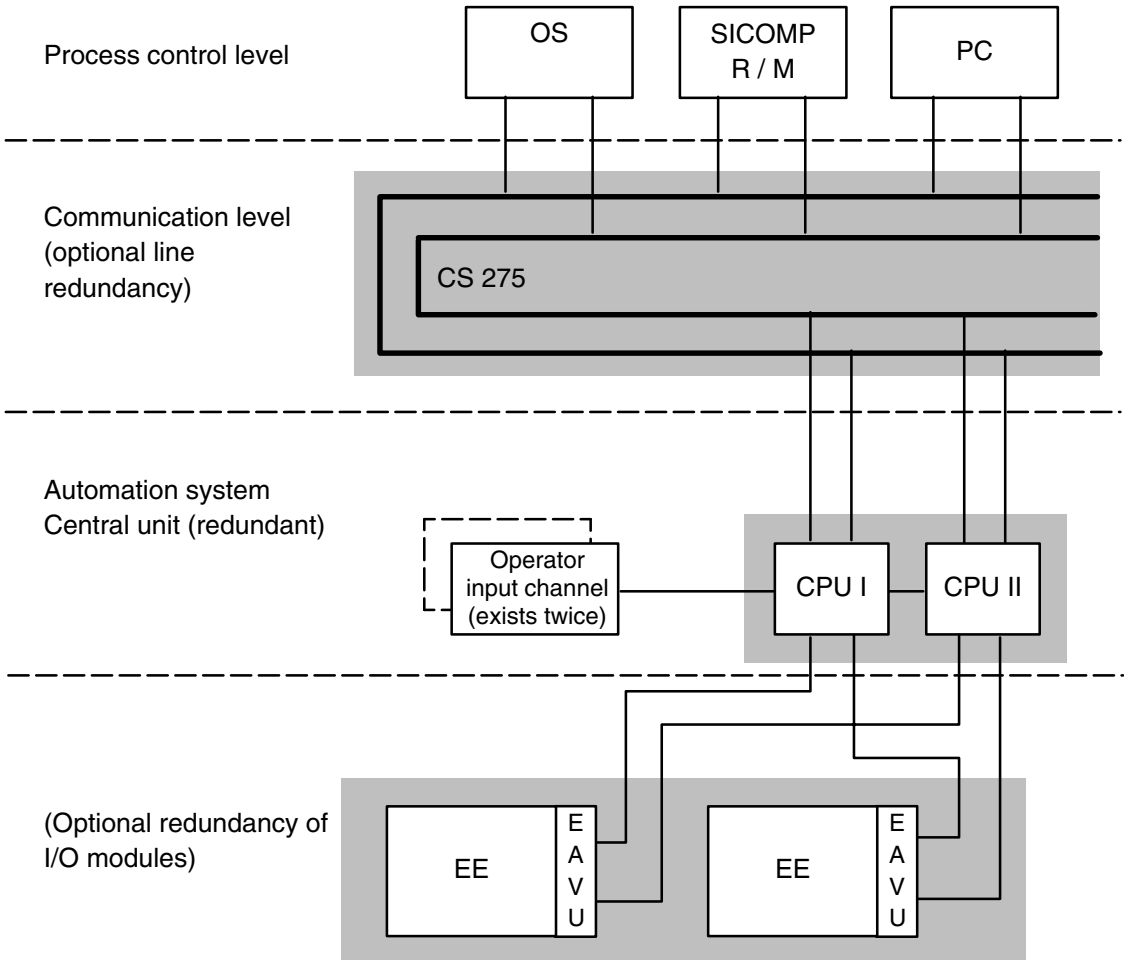
The I/O system may also be configured in a redundant manner (see Chapter 3). This is indicated by the two hatched extension units in Fig. 1.2. Fig. 1.2. shows a typical configuration, other structures are possible.

[1)] Redundancy (to DIN 4001) means that more resources per unit are available than are actually required for performing the specified task.



AF Remote bus connector board
SAE Cabinet connecting elements
VR Video relay
1 Power supply unit I (5 V)
2 Buffer module (24 V)
3 Power supply unit II (5 V)
4 Basic unit (ZE I + ZE II)
5 Extension unit (EE)
6 I/O comparator and switchover module
7 Cabinet power supply unit with:
– Circuit breakers
– Socket outlets
– Alarm logic modules
– Logic diode modules
– Cabinet power supply diode
– Inductive bus converter unit
– Blinking clock–pulse generator module
8 Group interrupt module (option)
9 Process cable clamping bar

Fig. 1.1 AS 235 H cabinet layout



OS	=	Operator control and monitoring system
SICOMP	=	SICOMP computer system
PC	=	Personal computer
CS 275	=	Bus system
ZE I	=	Central processing unit I
ZE II	=	Central processing unit II
EE	=	Extension unit
EAVU	=	I/O comparator and switchover module

Fig. 1.2 Redundant AS 235 H configuration

1.2 AS 235 H Modes

The following modes can be assumed by either central processing unit. Various combinations are possible.

Master (M)	The CPU has access to all its locally assigned modules. It is thus able to execute the application program in the same manner as a standard automation system. The mode of the second CPU may be: standby, backup, passive or failure.
Reserve (R)	CPU and master CPU execute all programs in synchronous operation (clock and instructions). The comparators on the comparator coupler module (VKB) and the I/O comparator and switchover modules (EAVU) monitor the data, address, and control signals for discrepancies. The standby CPU continues process execution in the event of a master CPU failure. The second CPU is in master mode.
Passive (P)	The CPU executes its program independently of the other CPU. Access to the CS 275 bus system and the I/O system are disabled by the hardware. The CPU has access to its local MDA and the BKAs. Monitors and printers are connected to the master CPU via an operator input channel switchover unit. Since the keyboards are connected to both CPUs, keyboard inputs are processed simultaneously by both CPUs. Keyboard inputs to the passive CPU, however, are not displayed. The connecting cables of configuring keyboard (not PBT) and monitor may temporarily be connected directly (without switchover function) to the passive CPU (for special tasks or maintenance purposes). Application program execution is halted when a CPU enters passive mode. The CPU assumes STO mode (block execution is halted). The mode of the second CPU may be: master, passive or failure.
Backup (B)	This mode indicates a transition from passive to standby mode. The passive CPU is first synchronized with the master CPU. Subsequently, the content of the user memory is transferred from the master CPU to the backup CPU. Application program execution is continued synchronously in both CPUs. The mode of the second CPU is, and remains, master.

Fault (F)

A CPU that has been identified as the cause of asynchronous operation between the two CPUs will assume failure mode. The CPU also assumes failure mode if a fault has been detected during start–up.

Although the CPU may still be operational it is not possible to establish synchronous operation between the CPUs (in contrast to passive mode). The CPU is also in failure mode after a power failure or a breakdown of a central module. The CPU is then no longer operational.

The cause of the failure can be determined by means of an information program (see Chapter 2.5.1.3). User program execution is stopped and the CPU assumes STO mode if a CPU enters failure mode after a malfunction has been located.
Once the fault has been repaired and the start–up selftest routine passed, failure mode can only be left by a restart (either central reset = ZRS or software reset = RSOF).

The mode of the second CPU may be: master, passive or failure.

The modes (except passive and failure) are independent of the STO (block execution halt) or STA (block execution start) modes. These modes only refer to **user program** execution.

STO mode is set when a CPU transitions to passive or failure mode. Since user program execution is not performed in this CPU, I/O access is not performed either. The latter would cause QVZ (time–out) and a corresponding I&C fault alarm.

Brief summary of the modes:

CPU I	CPU II	Explanations
M	R	Synchronous program execution
R	M	Synchronous program execution
M	B	Synchronization of CPU II, User program transfer to CPU II
B	M	Synchronization of CPU I, User program transfer to CPU I
M	P	Asynchronous operation User program is not executed in CPU II
P	M	Asynchronous operation User program is not executed in CPU I
M	F	Asynchronous operation: CPU II cannot be synchronized, start–up fault or power failure of module fault in CPU II
F	M	Asynchronous operation: CPU I cannot be synchronized , start–up fault or power failure or module faut in CPU I
P	F	User program is not executed in CPU I, start–up fault or power failure or module fault in CPU II
F	P	User program not executed in CPU II, start–up fault or power failure or module fault in CPU I
P	P	User program is not executed in CPU I and CPU II
F	F	Start–up fault or power failure or module fault in CPU I and CPU II

Table 1.1 Modes

1.2.1 Redundant Mode

Both CPUs operate synchronously (clock and instruction execution) in redundancy mode (M/R, R/M). The other CPU continues process execution if one CPU fails.

Synchronous operation also includes the M/B and B/M modes which are no redundant modes, however (see Chapter 1.2.2).

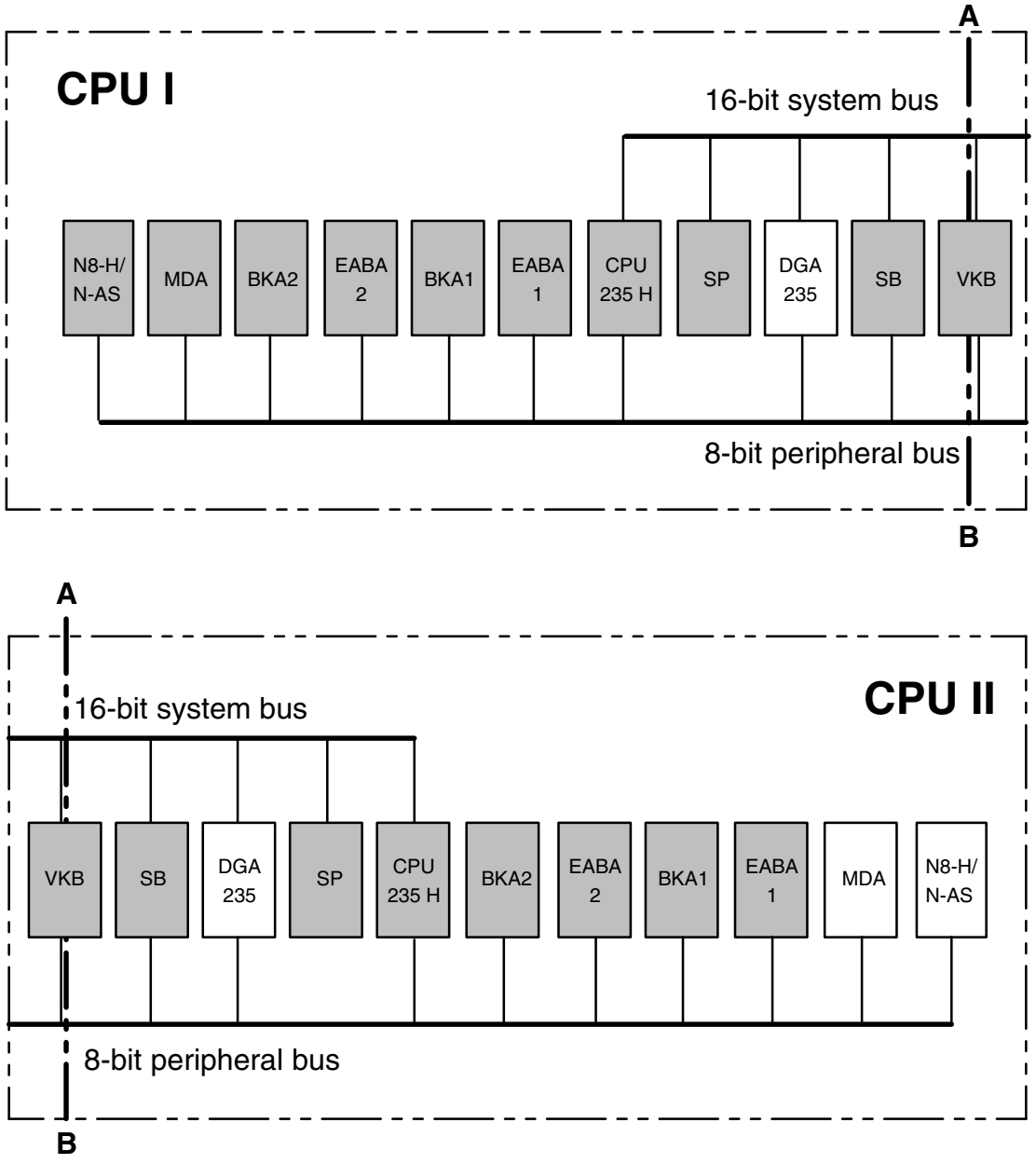
The comparator coupler module (VKB) in the central unit and the I/O comparator and switchover modules (EAVU) in th extension units monitor whether the bus signals to and from both CPUs are identical.

Fig. 1.3 shows the modules that are active in synchronous operation. It is assumed that CPU I is the master (see Chapter 1.2).

The clock pulse signals for the CPU modules are generated on the synchronization modules. The incoming control signals and clock pulses are synchronized on this module too.

The comparator coupler module monitors whether the control, data and address signals are identical in synchronous operation, and provides cross coupling of the N8–H and MDA access operations.

An interrupt signal is sent to each CPU if the modules detect a discrepancy between the bus signals in synchronous operation. The subsequent fault reaction is discussed in Chapter 4.2.



N-AS	Local bus interface module for automation systems
N8-H	Local bus interface module
MDA	Mini floppy disk interface module
BKA	Operator input channel interface module
EABA	I/O bus interface module
CPU	Central processing unit module
DGA 235	Diagnostic unit interface module
SB	Synchronization module
SP	Memory module
VKB	Comparator coupler module
ZE I	Central processing unit I
ZE II	Central processing unit II

Fig. 1.3 Synchronous operation of the AS 235 H central unit

1.2.1.1 Redundant Operator Input Channels

The following allocation is always valid in synchronous operation irrespective of the currently active master CPU. The necessary signal routing is performed by the comparator coupler module.

Keyboard inputs are entered in parallel into both CPUs.

The image output of an operator input channel is performed via the respective operator input channel interface module of both CPUs.

A switchover unit displays the BKA1 display contents of CPU I on the monitor of operator input channel 1.

Printer output of operator input channel is disabled by CPU II in BKA 1.
Printer output of operator input channel is disabled by CPU I in BKA 2.

1.2.1.2 Redundant I/O System

Two redundant I/O buses provide the connection to the extension units (EE) via the I/O comparator and switchover modules (EAVU) (see Fig. 1.2).
One redundant I/O bus is allocated to the extension units in the basic cabinet, the second I/O bus to the extension units in the extension cabinet.

The I/O bus **within** an extension unit is **not** redundant. Redundant configuration of the I/O system requires each redundant group of I/O modules to be accommodated in a different extension unit (see Chapter 3).

The I/O comparator and switchover modules guarantee that the connection between the master CPU and the extension units is maintained when one CPU or one I/O bus line fails.

In synchronous operation, read data is transferred to both CPUs simultaneously, whereas write command signals are transferred to the I/O modules from one CPU only. The signals are compared during read and write operations. An interrupt signal is sent to each CPU if the I/O comparator and switchover modules detect a discrepancy between the signals. The subsequent fault reaction is discussed in Chapter 4.2.

1.2.1.3 Redundant N8-H/N-AS Bus Interface Unit and Mini Floppy Disk Interface Module (MDA)

The following rules apply for synchronous operation:

Access to the CS 275 bus system and to the mini floppy disk unit (MDE) is performed via the respective N8–H/N–AS and MDA modules of the master CPU. The necessary signals for synchronous operation of the standby CPU are cross–coupled via the comparator coupler module (VKB).

The system recognizes a failure of the N8-H/N-AS module and transfers mastership to the other CPU (e.g. from M/R to R/M). This transfer selects the other N8-H/N-AS and MDA modules and initiates an I&C fault alarm (see Chapter 2.6.3). A malfunction of the N8-H/N-AS module is indicated by the I&C alarm S 374. The I&C alarm S 315 (DAUERDMA) signals a fault during N8–H/N–AS or MDA direct memory access.

The N8-H/N-AS module in the standby CPU processes selftest routines, and is parameterized by the CPU once mastership has been transferred to the second CPU.

Caution

A bus message may be lost during mastership transfer.

The optional line redundancy of the CS 275 bus system is independent of the interface redundancy. This means that the line redundancy is retained after a CPU failure, and vice versa.

1.2.2 Synchronous Operation

Synchronous operation includes redundancy mode (M/R and R/M) and the two temporary modes M/B and B/M. These two modes only differ from redundant mode in that the memory contents of the master CPU has not yet been transferred to the memory of the backup CPU.

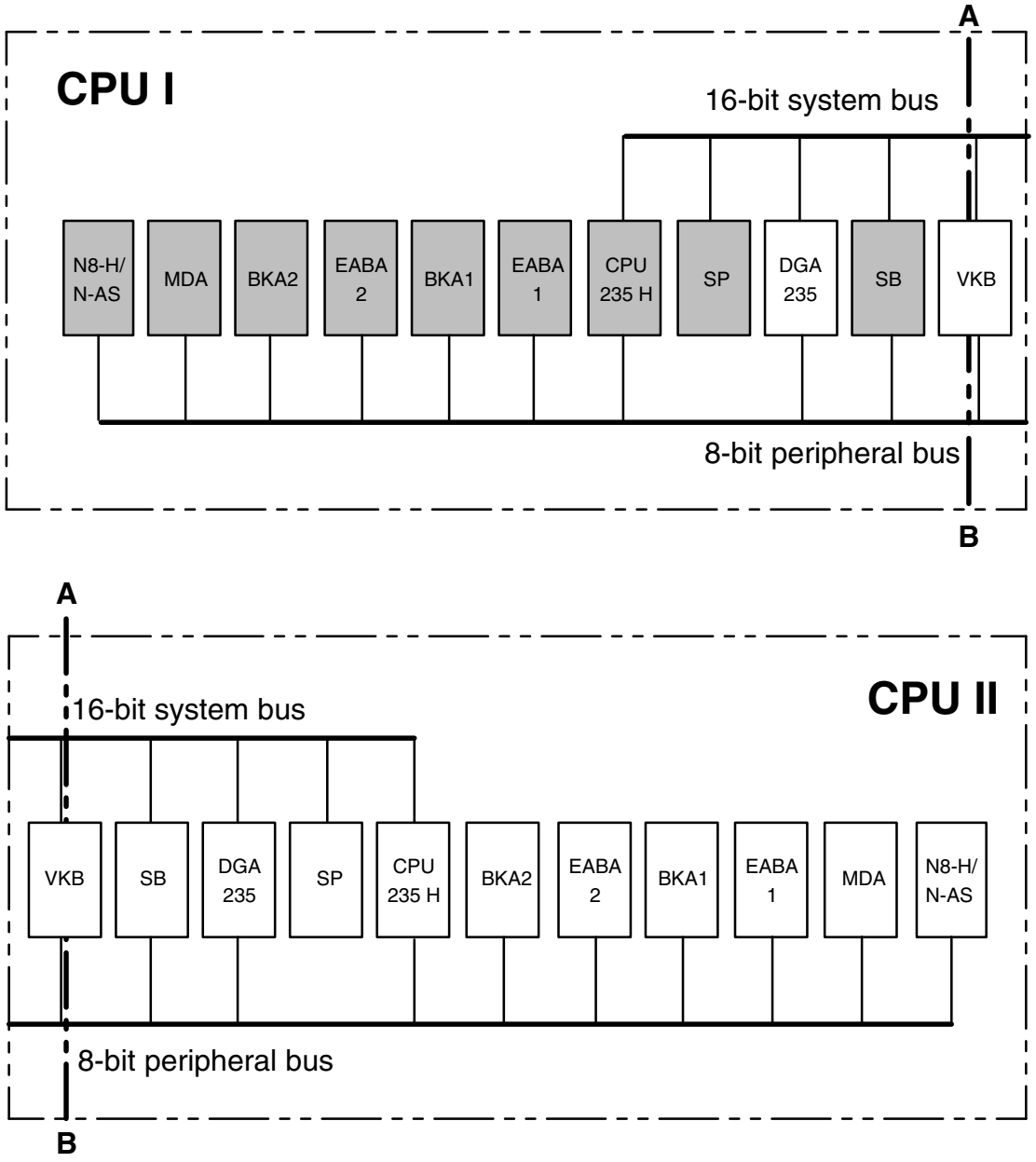
The two CPUs are already synchronous with regard to clock pulse and instruction sequence; the backup CPU, however, is not yet in a position to accept mastership in the event of a master CPU failure. Monitoring synchronous operation (i.e. monitoring the identity of the bus signals from and to both CPUs) is already performed by the VKB and EAVU modules during backup operation.

1.2.3 Asynchronous Operation

Both CPUs operate independently of each other in asynchronous mode. This means that they execute different instructions.

Asynchronous operation includes the M/P, P/M, M/F, F/M, P/F, F/P, P/P, and F/F modes.
Fig. 1.4 shows the active modules of CPU I in asynchronous mode; CPU I is master. The master CPU operates in the same manner as the central unit of a standard automation system. The synchronization module is solely used for generating the system clock pulse for the CPU. The comparator coupler module (VKB) is not required for asynchronous operation. The other CPU cannot influence the master CPU.

In order to restore the fault–tolerant features of the automation system, asynchronous operation should be terminated as soon as possible by synchronizing the passive CPU.



Hatched modules are active in asynchronous operation (CPU I is master here)

N-AS	Local bus interface module for automation systems
N8-H	Local bus interface module
MDA	Mini floppy disk interface module
BKA	Operator input channel interface module
EABA	I/O bus interface module
CPU	Central processing unit module
DGA 235	Diagnostic unit interface module
SB	Synchronization module
SP	Memory module
VKB	Comparator coupler module
ZE I	Central processing unit I
ZE II	Central processing unit II

Fig. 1.4 Asynchronous operation of the AS 235 H central unit

1.2.4 Operation as a Non–Redundant System

With a single central unit, the AS 235 H can be used as a non–redundant system. Compared with AS 235 Standard, such a system can easily be upgraded to a redundant system. Merely the missing modules in the central unit and the signalling logic module in the power supply tier need to be installed.

As a non–redundant system, the AS 235 H may be used with CPU I or CPU II. The mode after start–up is either M/F or F/M. The missing central processing unit (CPU II or CPU I) is thus treated as if it were defective or without power. The master CPU works in the same manner as the central unit of the standard AS. The statements made in this description for M/F or F/M mode and asynchronous mode apply.

1.3 Mode Transition

Figs. 1.5 to 1.8 show all possible mode transitions of an AS 235 H system. For clarity reasons they are illustrated in four different figures.

The operating state of both CPUs is always marked by a circle.

(M/P) for instance, means that CPU I is master and CPU II is passive

An arrow marks a status transition; the text next to the arrow indicates the cause of status transition.

The interim state P/P is represented as a dotted circle.

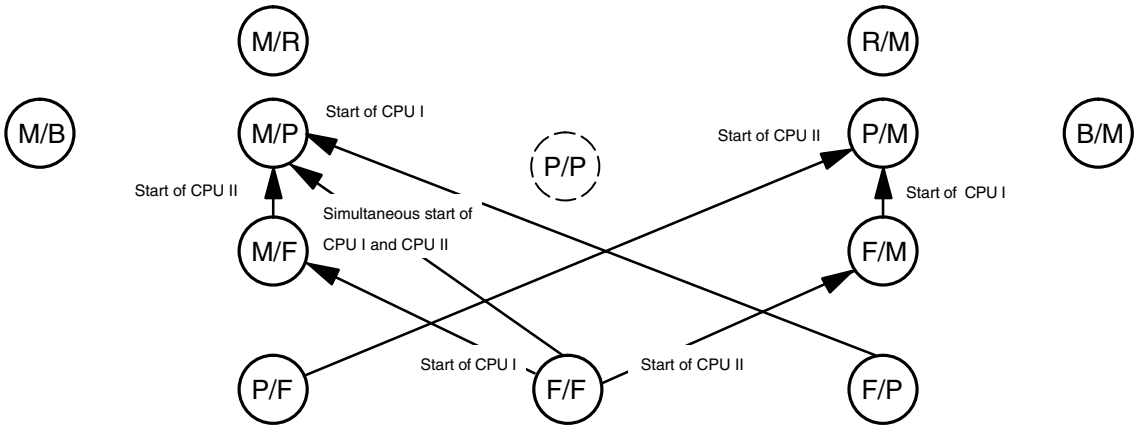
1.3.1 Mode Transition during Start–up (Fig. 1.5)

The start–up response is the same after a voltage recovery or after a central reset (ZRS). The starting CPU assumes mastership, unless the other CPU is master. In this case, the starting CPU becomes “passive”.

The starting CPU assumes failure mode if the selftest routine detects a malfunction during start–up. (This possibility is not depicted in Fig. 1.5)

CPU I becomes master if both CPUs are started simultaneously even if CPU II has a “lead” of less than one second. A lead of more than one second is no longer considered as a simultaneous start.

The mode is only changed after an RSOF or LOES keyboard command if the CPU mode was previously in failure mode. The mode is changed to “master” after the selftest routine has been passed if the other CPU was in passive mode (otherwise to “passive”).



M Master
R Standby
P Passive

B Backup
F Failure
M/R means: CPU I is master and CPU II is backup

Fig. 1.5 Mode transition during start–up

Note

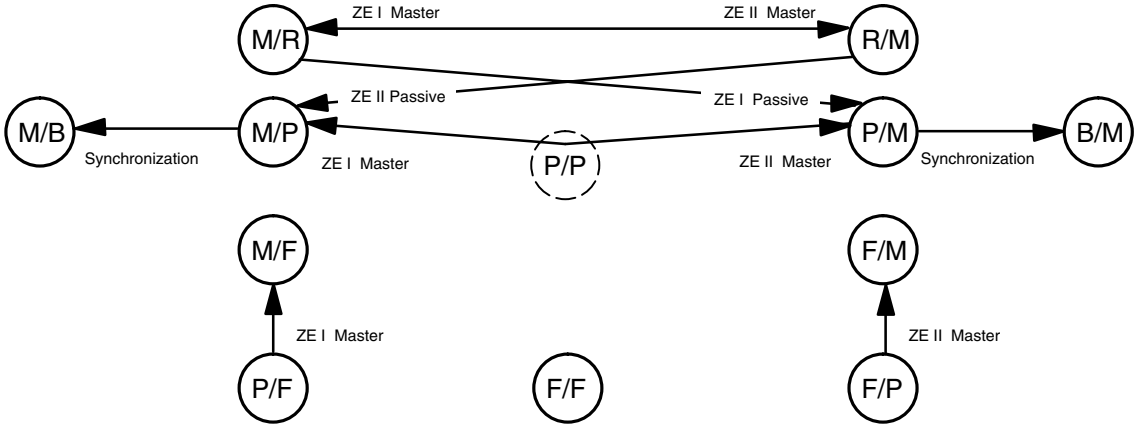
Power supply must be redundant. Mains failure in both CPUs is thus considered as a double fault. When both CPUs start up simultaneously, CPU I becomes master, not the CPU that was master before the mains failure.

1.3.2 Operator–Controlled Mode Transition (Fig. 1.6)

Apart from inputs that are required for synchronization, inputs are only permitted in STO mode. The transition from M/P to M/B or from P/M to B/M indicates the transition from asynchronous to synchronous mode. The mode changes from M/R to R/M once the user memory contents has been transferred from the master CPU to the backup CPU.

P/P mode is assumed briefly (for approximatel one second) as an interim state when the system transitions from M/P to P/M or vice versa. The reason is that the master CPU becomes passive first before the other CPU becomes master.

Possible operator inputs are discussed in Chapter 2.5.



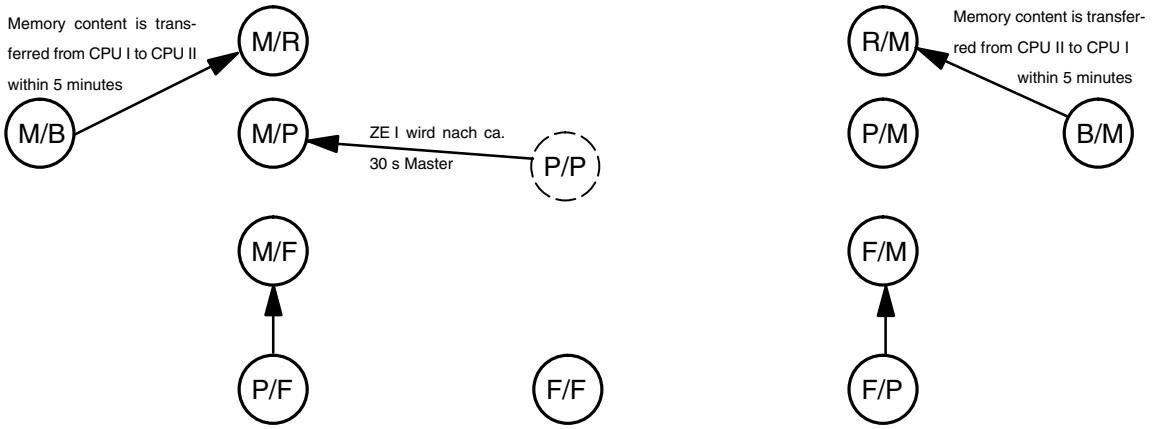
See Fig. 1.5 for legend

Fig. 1.6 Operator–controlled mode transition

1.3.3 Automatic Mode Transition (Fig. 1.7)

The system transitions from M/B or B/M to M/R or R/M once the complete user memory contents has been transferred from the master CPU to the backup CPU. A memory size of 3 MB takes approximately five minutes in STA mode or 40 seconds in STO mode. In STA mode, the user program execution is continued without interruption.

CPU I automatically assumes mastership if, due to a malfunction, the automation system remains longer than 30 seconds in P/P mode. User program execution is stopped for safety reasons; CPU I assumes STO mode.



See Fig. 1.5. for legend

Fig. 1.7 Automatic mode transition

1.3.4 Mode Transition after a Fault has Occurred (Fig. 1.8)

The fault can be a power failure, hardware failure or an actuated ZRS pushbutton.

Such a fault triggers the comparators on the comparator coupler module (VKB) or the I/O comparator and switchover modules (EAVU) which release an interrupt signal. Subsequently, both CPUs start executing diagnostics routines.

After the fault has been located, the CPU which caused the fault assumes “Failure” mode and the other CPU continues user program execution. The defective module must be replaced if the fault is a hardware fault.

The standby CPU assumes passive mode if the fault cannot be located, and the master CPU continues user program execution.

Subsequent automatic synchronization can be selected by parameterization. Mode transitions are indicated by I&C alarms.

Caution

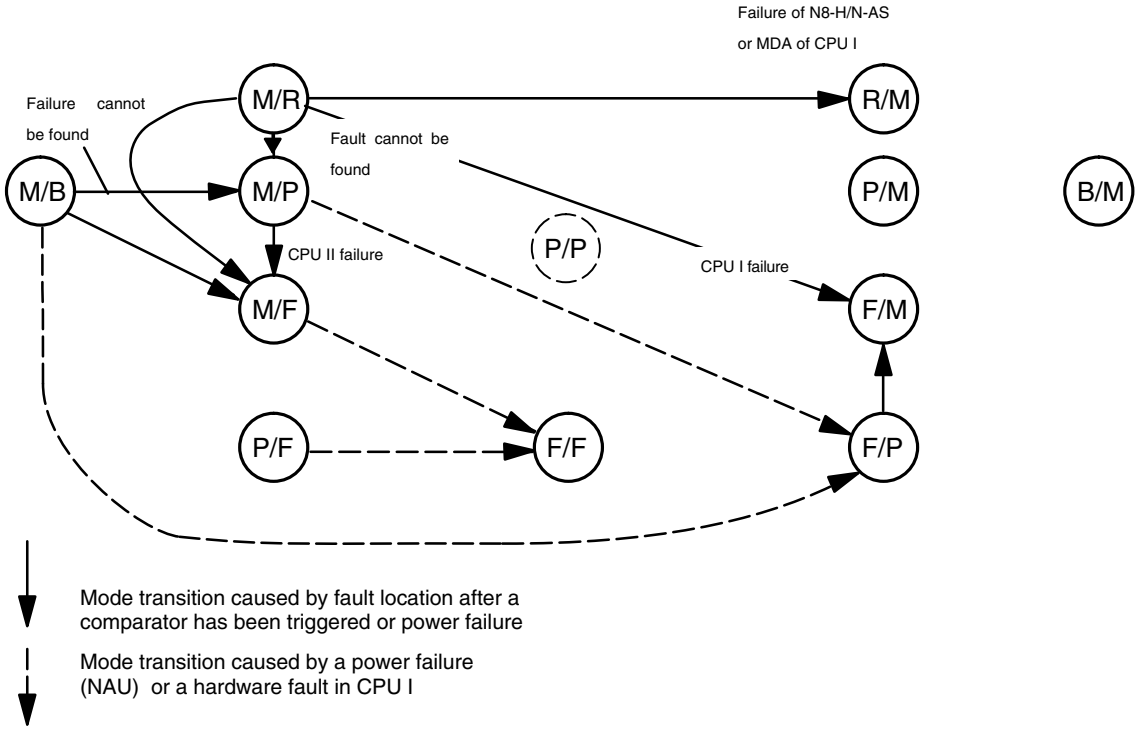
If a fault occurs during loading in synchronous mode (M/R, R/M, M/B or B/M), loading is aborted and a restart performed by the central processing unit which is not the master. In so doing, this central processing unit clears its user memory contents.

An exception are faults on N8-H/N-AS or MDA modules which do not trigger a comparator. Mastership changes if the N8–H/N–AS cannot be parameterized in M/R or R/M mode or if a DMA fault caused a permanently present DMA signal. Mastership is **not** changed again if the same fault also occurs in the other CPU.

One of the three I&C alarms S 315 (timing error, DAUERDMA), S 374 (N8–H/N–AS cannot be parameterized) or S 386 (N8–H/N–AS faulty) identifies the defect. Redundancy is maintained since process input/output can still be performed by both CPUs.

In order to preserve clarity, Fig. 1.8 only shows mode transitions that start from the left–hand side of the figure.

Corresponding mode transitions are also possible on the right–hand side of the figure, with the right and the left sides of the original reserved.



M Master
R Reserve
P Passive
B Backup
F Failure
M/R means: CPU I is master, CPU II is backup

Fig. 1.8 Mode transition after a fault has occurred

2 Method of Operation

2.1 Initial Loading of the System Software

Chapter 5 of the AS 235 H Operating Instructions (C79000-B8076-C293) describes the initial loading of the system.

The loading process is not displayed on the master CPU monitor during initial loading of a CPU: It may be displayed, however, if the monitor cable is connected to the BKA 1 of the CPU which is loaded. If no CPU is master, loading of CPU II can be monitored without changing cable connections. It is therefore recommended to start with CPU II if both CPUs are initially loaded from a floppy disk.

- On–line change of the system software

Chapter 2.5.1.1 describes how the system software can be changed without interrupting process execution.

User program execution, however, will be interrupted for approximately eight seconds (depends on the size of the user program structure).

Caution

Only the AS 235 H system software may be loaded.

2.2 Start–up Behavior (cf. 1.3.1)

A CPU first executes the RESTART blocks and then the user program if it becomes master during start–up and is in STA mode.

Cf. Chapter 2.3.8 of the AS 235 Variant G Description (C79000-T8076-C416).

2.3 Loading and Filing

Loading and filing of user programs takes place as described in the AS 235 Variant G Description (C79000-T8076-C416).

In asynchronous mode, each CPU loads and files only the memory contents of its own local memory module via its MDA. In synchronous mode, the contents of both memory modules (which are identical) are loaded and filed via the master CPU MDA (Cf. Chapter 2.5).

2.4 Synchronization

Synchronization of a passive CPU can either be started by pressing a pushbutton on the comparator coupler module (VKB) or by entering commands via the keyboard (see Chapter 2.5.1.1). The pushbutton must be pressed for approximately one second. (Unless the comparator coupler module (VKB) has been switched on there will be no reaction when the pushbutton is pressed). Provided that loading from the mini–diskette unit is not in progress, the two CPUs can only be synchronized if they are in M/P or P/M mode, and have the same module structure.

Both CPUs normally have the same memory size and software revision level (see Chapter 2.5.1.1). Synchronization is aborted and the cause indicated by an I&C alarm (LTM) if these requirements are not met (see Chapter 2.6.3, LTM 820 to 828). The mode transitions to M/B or B/M when synchronization is started. It changes to M/R or R/M once the user memory contents has been transferred from the master CPU to the backup CPU. Both CPUs operate in redundant mode, and have the same memory contents. The second CPU is able to continue user program execution and to assume mastership if the first CPU fails.
The backup process in STA mode takes approximately 1 minute and 40 seconds for 1 MB or approximately 5 minutes for 3 MB. In STO mode, 3 MB takes approximately 40 seconds. The back–up process in STA mode takes approximately 6 minutes and 20 seconds, and in STO approximately one minute if the memory module 6DS1844–8xy is used.
User memory transfer to the backup CPU requires additional execution time. Synchronization should therefore be omitted if cycle overload has occurred or is likely to occur.

See Chapter 2.6 for mode transition indication.

Caution

The following handling will delete the main memory contents in both central procesing units:
CPU I becomes master and CPU II becomes passive if both CPUs are reset by ZRS in B/M mode. As CPU I was previously in backup mode, its main memory content will be deleted during start–up. At this point in time, CPU II still contains its previous main memory content. If synchronization is now started in M/P mode, CPU II will absorb the blank memory content of CPU I. This means that the main memory content of CPU II will be deleted too.

2.5 Keyboard Input

Operator inputs in synchronous mode act upon both CPUs simultaneously.

Operator inputs in asynchronous mode also act upon both CPUs; they are executed by both CPUs but not at the same time. This can be achieved by connecting the keyboards via special cables (with three connectors) to both CPUs.
A switchover unit guarantees that, in asynchronous mode, the monitor always shows the master CPU display. In asynchronous mode, any actions of the passive CPU remain without effect to the master CPU and process execution.
Keyboard and monitor cables may be connected directly to the modules of a CPU (as with an AS 235 system) if the user wishes to utilize only one CPU for operator inputs and to have the screen contents of the CPU displayed, irrespective of the mode selected. This feature may be used for configuration changes during commissioning.
All operator inputs permitted for an AS 235 system are also possible for an AS 235 H system, and have the same effect.
Operator input to the AS 235 H system from a central configuration terminal via the CS 275 bus system is possible provided that one of the two CPUs is master and an N8–H/N–AS can thus be active.

2.5.1 Additional Operator Input and Help Programs

The SYST.HBED program enables H–related operator input and display programs to be started.

A program is called by the following input via the configuring keyboard:

```
SYST,HBED;
BE;
MP=no;
```

(no is the number of one of the subsequently displayed programs)

The following menu is displayed on the screen:

```
                BEDIENFUNKTIONEN AS235 H

     1 BEDIENUNG DES H-BETRIEBSZUSTANDS
     2 EAVU - ZUSTANDSANZEIGE
     3 HARDWARE-ANZEIGEN BEI SYNCHRONFEHLER
     4 EAVU-ANZEIGEN BEI SYNCHRONFEHLER
     5 SOFTWARE-ANZEIGEN BEI SYNCHRONFEHLER

                FUNKTIONSANWAHL MIT  MP = NR
```

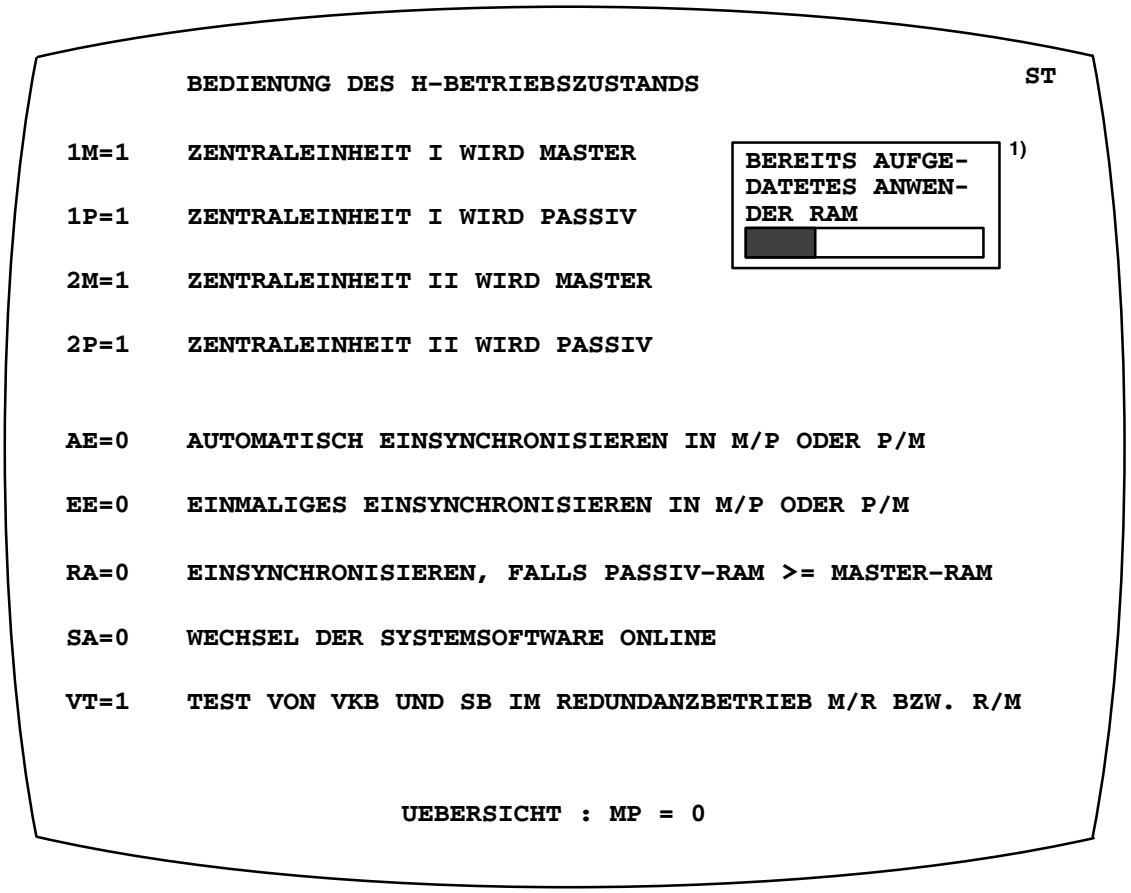
Fig. 2.1 Operator input function screen display

Caution

Parameters and variables of programs that have been linked with SYST.HBED are also transferred during filing from AS to floppy disk or during loading from floppy disk to AS, and remain unchanged.

2.5.1.1 H Mode Control

Enter MP=1 in SYST.HBED to select this screen form. The program is used for mode selection and parameterizing various system characteristics.



1) This window which displays the current updating level of the user RAM (and the system RAM after a system software change) is only displayed in the H modes M/B and B/M.

Fig. 2.2 Screen display containing the population of all possible indications in MP=1

- Mode selection

The parameters 1M, 1P, 2M and 2P are used for mode selection. Only such parameters are displayed which may be controlled in the currently selected mode. The related comments are always displayed for all parameters, irrespective of the mode selected.

This parameter may only be altered in STO mode, and may only be set to the value 1.

1M=1 CPU I becomes master

1M=1 is only permitted in STO mode and the states:

R/M (transition to M/R)
P/M (transition to M/P)
P/F (transition to M/F).

Transition in P/M operating state can only be controlled via the master CPU. The AS briefly selects P/P (for up to one second) if input is made in P/M state.

1P=1 CPU I becomes passive.

1P=1 is only permitted in STO mode and the states:

M/R (transition to P/M)
R/M (transition to P/M).

2M=1 CPU II becomes master

2M=1 is only permitted in STO mode and the states:

M/R (transition to R/M)
M/P (transition to P/M)
F/P (transition to F/M).

Transition in M/P operating state can only be controlled via the master CPU. The AS briefly selects P/P (for up to one second) if input is made in M/P state.

2P=1 CPU II becomes passive

2P=1 is only permitted in STO mode and the states:

M/R (transition to M/P)
R/M (transition to M/P).

Alterations of the parameters 1M, 1P, 2M and 2P that are not rejected are indicated by I&C alarms (see Chapter 2.6.3, LTM 812 to 817).

An illegal entry is rejected and the error message F 460 is issued. An I&C alarm is not issued.

- Automatic/one–time synchronization

AE Automatic synchronization [1)]

If **AE=1** (in the master CPU) synchronization always takes place in M/P or P/M mode, even after start–up of one or both CPUs. AE is set to zero if a fault occurs during synchronization. AE is also set to zero if **1P=1** or **2P=1** has been entered and the initial state was M/P or R/M.

The initialization value after a first–time run is **AE=1,** after memory clearing **AE=0**.

EE One–time synchronization [1)]

EE can only be altered in M/P or P/M state. If **EE=1** (in the master CPU) synchronization always takes place in M/P or P/M mode. EE is set to zero during synchronization (or when synchronization is aborted) or during start–up.

The initialization value after a first–time run or memory clearing is zero.

- Uprating the memory configuration in online mode

RA=0 Synchronization is not to be performed with different memory configurations.

Normally both central processing units have the same memory configurations, i.e. **RA=0** (no uprating)

RA=1 Synchronization is to be performed if the memory configurations differ

Using this parameter, the AS memory configuration can be uprated online. During synchronization with **RA=1** it has to be noted, however, that the memory size of the passive CPU **must** be larger than that of the master CPU.

Proceed as follows:

Switch off one CPU and uprate the memory module of this CPU to the memory capacity requested.
Switch on this CPU and bootstrap the system software.
Set **RA=1** to synchronize the CPU. Then switch off the second CPU and uprate its memory card as well. Switch on the second CPU and bootstrap the system software. Set **RA=1** to synchronize the CPU.

Uprating is finished now – both CPUs have been uprated – the uprate memory configuration is available now.

RA may only be altered in M/P or P/M states.

RA is set to zero during synchronization and when synchronization is aborted. Synchronization is aborted and an I&C alarm issued if the memory size of the passive CPU is smaller than the memory size of the master CPU (see Chapter 2.6.3).

The initialization value after a first–time run or memory clearing is zero.

[1)] There will be no reaction to the AE and EE parameters unless the comparator coupler module (VKB) has been switched on.

- Upgrading the system software

SA=0 Synchronization is not to be performed with different system software versions.

SA=1 Synchronization is to be performed with different system software versions. The software version of the passive CPU is to be adopted in both CPUs.

SA is set to zero during synchronization and when synchronization is aborted. SA may not be altered in M/B or B/M state. The initialization value after a first–time run or memory clearing is zero. How to proceed during a system software change is described in the below examples.

A bumpless change (with regard to the process variables) from one system software version to another is possible if the process tolerates a dead time of approximately 8 seconds during execution level stop and subsequent restart. (The restart which is always necessary after a new system software version has been loaded is performed automatically).

The watchdogs of the I/O bus interface units are triggered during start–up. The outputs of the output modules (analog/binary) are not reset. The control module watchdogs, however, are not triggered during start–up. The cycle–time of the control module watchdogs must be set to its maximum value (16 seconds) before the system software is changed. A shorter cycle time may be selected once the system software has been changed. RESTART blocks are not processed during this special start–up.

The time is reset after start–up (as after ZRS). Bus messages may be lost as the N8–H/N–AS is parameterized during start–up. The specified duration of 8 seconds is an average value which depends on the size of the user structures.

Caution

Proper program continuation is not guaranteed if a system software change is interrupted by NAU, ZRS, RSOF, LOES, or loading from floppy disk or bus.

- Examples of a system software change:

CPU I executes the user program with system software version X (CPU II: standby or passive).

1) CPU II is to be booted with system software version Y:

   Set the switch on the memory module front panel to BOOT and press the ZRS push–button on the CPU front panel at the same time.

   CPU II performs loading and assumes passive mode

2) The following inputs enable synchronization:

```
SYST,HBED;
BE;
MP=1;
SA=1;
```

   The CPU status has not yet changed.

3) Synchronization via keyboard

   Input: **`EE=1;`** or **`AE=1;`**

   Synchronization is also possible by pressing the BU pushbutton on the VKB front panel.

The subsequent transfer of the user memory contents from CPU I to CPU II is performed while CPU I and CPU II execute the user program in synchronous operation (using system software version X).

Sequence list execution is stopped at the end of the lists when this process is terminated. The user program assumes a defined state. Both units briefly transition to STO mode. The watchdogs of the I/O interface modules are triggered during this process (see above).

CPU I automatically assumes passive mode now. CPU II, the new master, uses the new system software Y for performing a restart, and transitions to STA mode (provided that STA was the mode before the change).

From now on, system software version Y is used for executing the user program.

CPU I is now synchronized automatically. The system software (version Y) and the user memory contents are the transferred from CPU II to CPU I. Both CPUs utilize the new system software Y.

If there is a restart due to a change in master while the operator is entering configuration data via the bus system, the bus connection will be interrupted. The bus connection can be set up again by signing off and then on again.

The appendix contains the upgrading instructions for the memory module 6DS1844–8xy and system software version G.

- Testing the comparator

`VT=1` The comparator coupler module (VKB) and the synchronization module are tested in redundant mode (M/R or R/M).
This parameter is only required by system specialists who use logic analysers for performing certain hardware tests while **`VT=0`**. This parameter should be 1 in normal operation.

All possible operator inputs are displayed on the process communication keyboard (PBT). Dynamic PBT annotation is not performed.

2.5.1.2 EAVU Status Display

This SYST.HBED screen form is selected by **MP=2**. This program displays the EAVU functions, the allocation of the EAVU modules to the slot addresses of the I/O modules, and to the words 0 to 2 (alarms 1 to 48) of the 6DS1601–8BA interrupt module.

Example:

```
                    EAVU-ZUSTANDSANZEIGE

            EAVU - ZUSTAND IM GRUNDSCHRANK

EAVU | EIN/AUS |        STECKPLATZADRESSEN          | INT-ADR.
-----------------------------------------------------------
 0   |   EIN  |  0-11                              | 0   D
 1   |   EIN  |        16-27                       |   1    H
 2   |   EIN  |                  32-43             |      2   S

      EAVU - ZUSTAND IM ERWEITERUNGSSCHRANK

EAVU | EIN/AUS |        STECKPLATZADRESSEN          |
-----------------------------------------------------------
 100 |   EIN  | 100-111                            |
 101 |   AUS* |                  132-143           |
 102 |   AUS  | 100-111  116-131                   |
 103 |   AUS  | BR.I(08H) UNGLEICH  BR.II(09H)     |

     IS=2   SW=INTERRUPTSPERRE SETZEN BEI EAVU NR (GS)
     IF=0   INTERRUPT FREIGEBEN BEI EAVU NR (GS)

                    UEBERSICHT : MP = 0
```

Interpretation:

EAVU 0 This module is installed in the basic cabinet; has been switched on; is responsible for slot addresses 0 to 11 and primarily responsible for word 0 (alarms 1 to 16) of the group interrupt module; one interrupt is pending for a too long time.

EAVU 1 This module is installed in the basic cabinet; has been switched on; is responsible for slot addresses 16 to 27 and primarily responsible for word 1 (alarms 17 to 32) of the group interrupt module: too many interrupts have occurred.

EAVU 2 This module is installed in the basic cabinet; has been switched on; is responsible for slot addresses 32 to 43 and primarily responsible for word 2 (alarms 33 to 48) of the group interrupt module; the interrupts were inhibited via keyboard operation.

EAVU 100 This module is installed in the extension cabinet; has been switched on; is responsible for slot addresses 100 to 111.

EAVU 101 This module is installed in the extension cabinet; has been switched off by an EAVU driver block (PRS signal of the EAVU driver is 1); is responsible for slot address 132 to 143 when it is switched on.

EAVU 102 This module is installed in the extension cabinet; has been switched off by the system software as the slot address responsibility was overlapping with EAVU 100 (slot addresses 100 to 111 have been selected again).

EAVU 103 This module is installed in the extension cabinet; has been switched off by the system software as jumper register I (value 08H) and jumper register II (value 09H) are not identical (jumper register I states that the EAVU is responsible for slot addresses 148 to160; jumper register II implies additional responsibility for slot addresses 100 to 111)

Fig. 2.3 EAVU screen display

The system software performs a check in order to be able to create the EAVU status display. This check is performed for all EAVU modules after each master CPU start–up (power ON, ZRS or RSOF); it is only locally performed if the power is switched on for an extension unit only.

The check is performed as follows:

The QVZ signal that results from an EAVU access is used for creating the information whether or not the I/O comparator and switchover module (EAVU) has been installed. Subsequently the jumper settings I and II on the EAVU are checked for identity. These settings, which should be redundant, specify the slot addresses of the I/O modules and the group interrupt module the EAVU is responsible for. The checked EAVU is switched off and the I/O modules of the extension unit containing the EAVU are reset if the jumper settings are not identical or if they overlap with the setting on a previously checked EAVU. EAVU 102 of the example on the previous page was switched off since its responsibility for slot addresses 100 to 111 was overlapping with the responsibility of EAVU 100. The exact reaction with regard to the I/O module is as follows:

– The outputs of the output modules (binary/analog) are reset (depending on the ARS jumper)
– The closed–loop control modules change from mode C (compute) to mode A (automatic)
– 2–channel closed–loop control modules, backplane connector 2, CB signal to 0

The EAVU is switched on and the reset signal for the I/O modules de–activated if the jumper settings are identical and do not overlap with a previously checked EAVU.
The check of the EAVU jumper settings follows the ascending EAVU numbers.
It takes the system software approximately 8 seconds to detect that the power supply of an extension unit has been switched off.

The EAVU driver block offers further display and control functions for the EAVU (see Chapter 3.2.2). The EAVU is switched off if the peripheral reset signal has been issued via the EAVU driver (PRS input of the EAVU block is 1). This is marked by an asterisk (*) next to “AUS” [OFF] in the above table. The EAVU remains de–activated (even after power off, ZRS, or RSOF) in this case until it is re–activated by an EAVU driver (PRS input of the EAVU block is 0; cf. Chapter 3.2.2).

Caution

An EAVU remains de–activated if the EAVU driver which has issued the peripheral reset signal for this EAVU is cleared. It can only be re–activated by an EAVU driver which cancels the reset signal for this EAVU.

2.5.1.3 Hardware Flags after Synchronization Faults

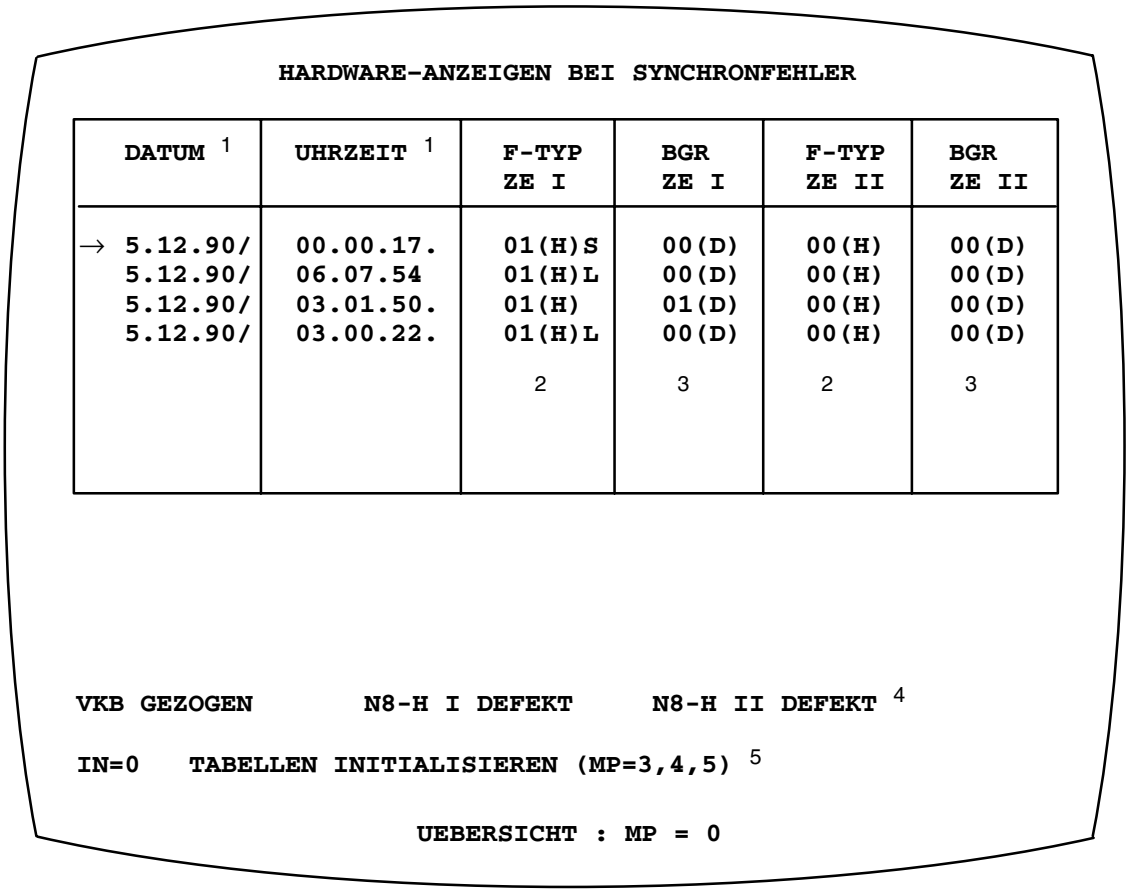
Selecting **MP=3** in SYST.HBED activates this screen display. This program displays the fault states of CPU I and CPU II. The last 10 events, together with date and time, are retained in a table. The values determined by the hardware can be displayed for both CPUs (see Fig. 2.4).

The fault type (F–TYP) specifies during which type of access the fault has occurred. The contents of VKB register 1 is displayed as a hexadecimal value (e.g. 01(H)S means “asynchronous memory bus during write operation”). An L or S at the end indicates whether the fault has occurred during a read (L) or a write (S) operation; an N at the end indicates an N8–H/N–AS fault. The following table summarizes the meanings of the individual bits of this value:

Reading (MEMR) the fault type

Address	Bit (1-active)	Meaning
4FD0H	0	Asynchronous memory bus
	1	Asynchronous peripheral bus
	2	Fault on memory data bus
	3	Fault on peripheral address bus
	4	Fault on peripheral data bus
	5	Fault in I/O area 1
	6	Fault in I/O area 2

Table 2.1 VKB register 1



HARDWARE–ANZEIGEN BEI SYNCHRONFEHLER

	DATUM [1]	UHRZEIT [1]	F-TYP ZE I	BGR ZE I	F-TYP ZE II	BGR ZE II
→	5.12.90/	00.00.17.	01(H)S	00(D)	00(H)	00(D)
	5.12.90/	06.07.54	01(H)L	00(D)	00(H)	00(D)
	5.12.90/	03.01.50.	01(H)	01(D)	00(H)	00(D)
	5.12.90/	03.00.22.	01(H)L	00(D)	00(H)	00(D)
			2	3	2	3

VKB GEZOGEN **N8-H I DEFEKT** **N8-H II DEFEKT** [4]

IN=0 TABELLEN INITIALISIEREN (MP=3,4,5) [5]

UEBERSICHT : MP = 0

1 The synchronization date and time entered in this display line are also valid for the corresponding display line in the screen from “Software–Anzeigen bei Synchronfehler” (Software flags after synchronization faults), (MP=5 in SYST.HBED).

2 See table 2.1.

3 The module which was addressed by the respective CPU at the moment when the fault occurred is shown (as decimal value) in the columns BGR ZE I and BGR ZE II (module CPU I and module CPU II). See table 2.2 for the meaning of the decimal values (0 to 27).

4 Indication is given if the comparator coupler module (VKB) has been removed (only then) or one (or both) N8–H/N–AS module(s) are defective. A permanent DMA signalled by I&C alarm DAUERDMA*S315 can also mean that the MDA is defective.

5 The IN parameter is used for clearing the entries for F–TYP and BGNR (IN=0 or IN=1) from the table. All ten lines of the display and screen forms “EAVU Anzeigen bei Synchronfehler” (MP=4) (EAVU flags after synchronization faults) and “Software Anzeigen bei Synchronfehler” (MP=5) (Software flags after synchronization faults) are cleared then.

Fig. 2.4 Hardware flags after synchronization faults

Module	Mo. type dec.	Register 2: Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Hexadecimal Addresses	Comment
	0	0	0	0	0	0		No module addressed
EABA1	1	0	0	0	0	1	PESPA#FDD,	Module was addressed at fault time
EABA2	2	0	0	0	1	0	PESPA#FDD,	Module was addressed at fault time
BKA 1	3	0	0	0	1	1	PESPA#FCX & ADB13=0, PESPA#F8X & ADB13=0,	Module was addressed at fault time
BKA 2	4	0	0	1	0	0	PESPB#FCX,PESPA#F8X & ADB13=1,	Module was addressed at fault time
VKB	5	0	0	1	0	1	PESPB#FD#00XX,PESPB#FD(0111)7,	Module was addressed at fault time
SB	6	0	0	1	1	0	PESPB#FD#00XX,PESPA#FD7,	Module was addressed at fault time
EAVU-1-0	7	0	0	1	1	1	PESPA#F7X,	Module was addressed at fault time
EAVU-1-1	8	0	1	0	0	0	PESPA#F6X,	Module was addressed at fault time
EAVU-1-2	9	0	1	0	0	1	PESPA#F5X,	Module was addressed at fault time
EAVU-1-3	10	0	1	0	1	0	PESPA#F4X,	Module was addressed at fault time
EAVU-2-0	11	0	1	0	1	1	PESPB#F7X,	Module was addressed at fault time
EAVU-2-1	12	0	1	1	0	0	PESPB#F6X,	Module was addressed at fault time
EAVU-2-2	13	0	1	1	0	1	PESPB#F5X,	Module was addressed at fault time
	14	0	1	1	1	0		VKB defective
EAVU-2-3	15	0	1	1	1	1	PESPB#F4X,	Module was addressed at fault time
INT-BE	16	1	0	0	0	0	PESPA#F4#0XXX,	Module was addressed at fault time
	17	1	0	0	0	1		VKB defective
	18	1	0	0	1	0		VKB defective
	19	1	0	0	1	1		VKB defective
EA-1 =E/A-area 1	20	1	0	1	0	0	PESPA#F__NXX,PESPA#F#00XX#X,	Module of area was addressed at fault time
	21	1	0	1	0	1		VKB defective
	22	1	0	1	1	0		VKB defective
	23	1	0	1	1	1		VKB defective
EA-2=E/A-area 2	24	1	1	0	0	0	PESPA#F__NXX,PESPA#F#00XX#X,	Module of area was addressed at fault time
	25	1	1	0	0	1		VKB defective
	26	1	1	0	1	0		VKB defective
	27	1	1	0	1	1		VKB defective

= delimiter

Table 2.2 Addressed modules at fault time

2.5.1.4 EAVU Flags after Synchronization Faults

Selecting **MP=4** in SYST.HBED activates this screen display. The master CPU only reads and stores registers 4 to 7 on all EAVUs when the CPU operation starts to be asynchronous. The register contents can be helpful for fault analysis (see Chapter 4.4).

This program is used for displaying the stored values. Since the register values are stored by the master CPU only, only the master CPU can display these values. The values are displayed in hexadecimal representation.

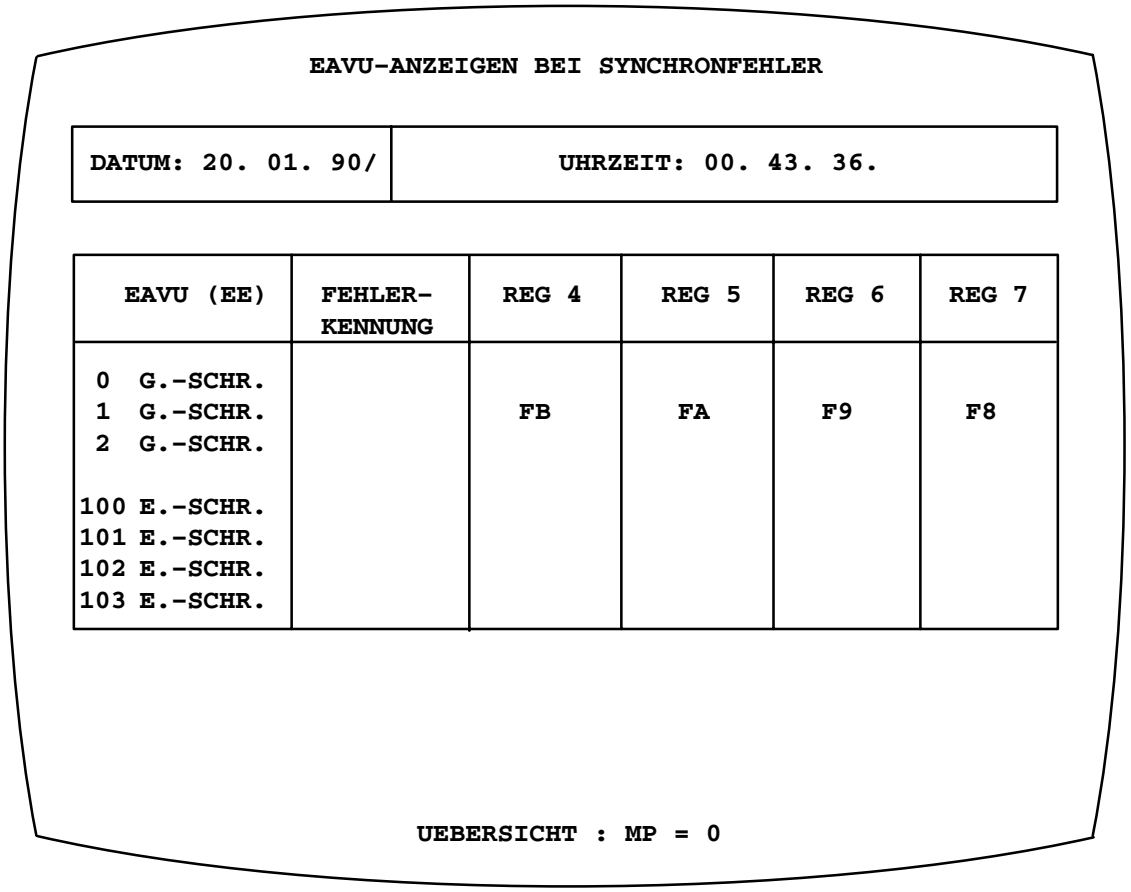


Fig. 2.5 EAVU flags after synchronization faults

If **IN=0** or **IN=1** has been entered for clearing the values from the screen form “Hardware flags after synchronization faults” (**MP=3** in SYST.HBED), the screen forms “EAVU flags after synchronization faults” (**MP=4** in SYST.HBED) and “Software flags after synchronization faults” (**MP=5** in SYST.HBED) are cleared too.

2.5.1.5 Software Flags after Synchronization Faults

Selecting **MP=5** in SYST.HBED activates this screen display (see Fig. 2.6 on page 2-16).

This program is used for displaying

– the states of CPU I and CPU II at the time when the synchronization fault has occurred;
– the fault finding results of CPU I and CPU II
– possible start–up faults of CPU I and CPU II (nothing will be displayed if start–up faults have not been detected).

A table shows the last ten synchronization faults together with the states that have been determined by the software and the recognized malfunctions. The information in the “Hardware flags after synchronization faults” screen (**MP=3** in SYST.HBED) and the infomation in this screen form always belong together if they are located on the same line of the respective table. Date and time of a display line can thus be retrieved from the corresponding line of the “Hardware flags after synchronization faults” screen.

The states of the last synchronization fault to have occurred are located on the topmost line of the table (indicated by a preceding arrowhead).

The “TYP–NAME”, ..., “VKB–REG. ADR.–BUS” columns must be used for interpretation if neither the “FEHLER ZE I” [fault CPU I] nor the “FEHLER ZE II [fault CPU II] column of a displayed line contains a value that is different from 00.
Such an interpretation requires special knowledge and can therefore only be done by a system expert.

The “EAVU flags after a synchronization fault” (**MP=4** in SYST.HBED) and “Software flags after a synchronization fault” (**MP=5** in SYST.HBED) are also cleared if the flag has been deleted from the “Hardware flags after a synchronization fault” (**MP=3** in SYST.HBED) screen form by **IN=0** or **IN=1**.

Example:

SOFTWARE–ANZEIGEN BEI SYNCHRONFEHLER

FEHLER ZE I	FEHLER ZE II	TYP- NAME	BST- NAME	RELATIV ADRESSE	EBENE	PAR	VKB–REG. ADR.–BUS
→ 31	00	SYST	HVER	10978	14	8FD7	01F3C200
1	1	2	2	3	4	5	6

ANLAUF–FEHLER ZE I : 02 [7]

ANLAUF–FEHLER ZE II: 02 [7]

UEBERSICHT : MP = 0

1 The software fault locating results of CPU I (II) are displayed here according to Table 2.3.

2 Type and block name of the block that was executed when the synchronization fault occurred.

3 The “RELATIV ADRESSE” [relative address] column specifies the decimal value of the address (relative to the block body) of the instruction that immediately follows the instruction that was executed when the synchronization fault occurred.

Caution

If a program is modified that is listed in the “Software flags after synchronization faults”, the corresponding flags in the “RELATIVE ADRESSE” [relative address] column may point to the wrong commands after this modification has been made. A program modification becomes effective after:
– program re–compilation
– a new system software version has been loaded

4 The execution layer displayed here was active when synchronization fault occurred.

5 This column shows the hexadecimal value of the content of the I/O address register of the execution layer that was active when the synchronization fault occurred (”EBENE” [layer] column).

6 This column is only relevant if the entries in the screen form “Hardware flags after synchronization faults” (**MP=3** in SYST.HBED) indicate a fault of the memory bus. It contains the start address of a 512–byte memory area that is stored in the VKB registers 3 and 5 (see VKB description C79000-T8076-C345). The CPUs became asynchronous during an access to this area.

7 This line is only displayed if CPU I (II) has detected a malfunction after start–up (ZRS or RSOF or LOES or after loading).

Fig. 2.6 Software flags after a synchronization fault has occurred.

Ident.	Fault type
00	No fault
01	VKB has been removed
02	Memory fault (parity fault or illegal instruction)
03	Fault on operator input channel interface 1
04	Fault on operator input channel interface 2
05	Fault on EAVU 0 (basic cabinet)
06	Fault on EAVU 1 (basic cabinet)
07	Fault on EAVU 2 (basic cabinet)
08	Fault on EAVU 3 (basic cabinet)
09	Fault on EAVU 100 (extension cabinet)
10	Fault on EAVU 101 (extension cabinet)
11	Fault on EAVU 102 (extension cabinet)
12	Fault on EAVU 103 (extension cabinet)
13	Primary fault (power failure)
14	Microprogram indication: – Allocation code violated, or PROM write protection, or type error during variable access, or fixed point overflow, or exponent overflow/underflow, or division by zero. This indication, which may be helpful for diagnostic purposes, does not initiate failure mode.
15	I/O bus interface module in basic cabinet is defective
16	I/O bus interface module in extension cabinet is defective
17	Comparator coupler module (VKB) is defective
18	EAVU 0 (basic cabinet) has been inserted (cable connected at one end only)
19	EAVU 1 (basic cabinet) has been inserted (cable connected at one end only)
20	EAVU 2 (basic cabinet) has been inserted (cable connected at one end only)
21	EAVU 3 (basic cabinet) has been inserted (cable connected at one end only)
22	EAVU 100 (extension cabinet) has been inserted (cable conn. at one end only)
23	EAVU 101 (extension cabinet) has been inserted (cable conn. at one end only)
24	EAVU 102 (extension cabinet) has been inserted (cable conn. at one end only)
25	EAVU 103 (extension cabinet) has been inserted (cable conn. at one end only)
26	Incorrect memory configuration of system or user RAM
27	Memory fault during memory test
28	Synchronization module (SB) is defective
29	CPU was in backup mode
30	Fault on N8-H/N-AS
31	Bus connector of local bus interface module has been removed

Table 2.3 Fault types

2.6 H Mode Indication

2.6.1 LEDs on H–related Modules in the Central Unit

Four LEDs on each synchronization module indicate the modes of the individual CPUs. One of two green LEDs is ON if the CPU is in master or standby mode. A yellow LED indicates that the CPU is in passive mode.
The associated CPU is in backup mode if the standby **and** passive LEDs are both ON.
A red LED indicates failure mode. This state can only be changed by repair or a restart (ZRS or RSOF). The master CPU is not influenced by this state.
All LEDs are OFF for approximately 1 second during start–up.

2.6.2 Displays

Two characters in columns 35 and 36 of line 30 indicate the modes of both CPUs (M/R, M/P, M/B, R/M, P/M, B/M, F/M, P/P, P/F, F/P, F/F). The following colours are used for display:

- M/R and R/M: black on green
- M/B and B/M: black on yellow, blinking
- M/P, P/M, M/F and F/M: from master CPU: black on yellow
  from the non–master CPU: black on white
  The different colours (yellow or white) indicate whether the screen contents refers to the master CPU or the non–master CPU.
- F/P, P/F, P/P and F/F: black on red

2.6.3 H–related I&C Alarms (LTM)

The I&C alarms S 800 to S 899 are only possible in an AS 235 H system. These H–related alarms are output on the AS monitor, on the AS event recorder and, via the CS 275 bus system, on the operator control and monitoring system (OS).

I&C alarms indicate the following events:

– mode change
– operator input
– cause for aborting synchronization
– fault

- Mode change indication

The I&C alarms S 800 to S 811 signal a mode change. The alarm number issued after a mode change tells the new mode. The alarm text shows the old and the new mode.

Example: MR → RM * S 804 enables acknowledgement for the I&C alarm S 800. S 800, since the previous mode was M/R.

The consequence of this is that **any** change in a sequence of mode transitions is reported.

- Output of H operating states on the OS

The current operating state of the AS 235 H can **be** displayed on the OS by entering the following command:

```
QF,*,800,811;
```

This entry is possible via the syntax **`QF,BTYP,BSNR,FENR;`** whereby an * can be entered as BTYP, 800 as BSNR and 811 as FENR).

As only the last I&C alarm of a mode change is available, the current operating state of the AS 235 H can be determined by means of this I&C alarm (see table 2.4).

Using the same syntax (**`QF,*,NR1,NR2;`**) the operator can have displayed any group of I&C alarms. The I&C alarms from NR1 to NR2 are displayed. The entire H–related I&C alarms can be displayed using the command:

```
QF,*,800,899;
```

- Operator input indication

Any operator input that causes a mode transition is indicated by one of the I&C alarms S 812 to S 819. In asynchronous mode, the operator input is only indicated by the CPU which performs it. Operator input indications enable acknowledgement for themselves. The sequence of repeated operator inputs can thus be reconstructed on the printout.

The alarms S 812 to S 829 are self–acknowledging; acknowledgements need not be enabled.

- Indication of synchronization start

The I&C alarms S 816 and S 817 indicate whether synchronization has been started by pressing the pushbutton on the comparator coupler module (VKB) or via the keyboard.

- Indication of synchronization abortion

The I&C alarms S 820 to S 826 indicate why synchronization has been aborted.

- Start–up indication

The I&C alarm S 827 is used for indicating start–up after an on–line system software change.

- Synchronization with different user memory configuration

I&C alarm S 828 indicates that both CPUs have been synchronized, although the memory of the passive CPU was larger than the memory of the master CPU.

- Fault indication

The I&C alarms S830 to S839 indicate EAVU faults. The number of the faulty I/O comparator and switchover module (EAVU) is displayed in plaintext. The I&C alarms from S 840 onwards indicate further faults that have been determined by the test routines. The operator must acknowledge fault alarms.

- Deviation from AS 235 standard

I&C alarm S 357 (backup battery discharged) in synchronous operation means that one of the backup batteries on the memory modules is empty. **Both** batteries must be replaced in this case.

Number	Text	Explanation
		x in the following alarm texts indicates the EAVU number (x = 0 to 3), y indicates basic cabinet (y = G or extension cabinet (y = E).
S 305	EAVUx yS	Time–out on an EAVU that has previously acknowledged
	UHR I	Real–time clock on memory module of CPU I defective
	UHR II	Real–time clock on memory module of CPU II defective
S 323	AUSF INT	Failure of a redundant group interrupt module
S 325	EAVUx yS	EAVU was de–activated by an EAVU driver
S 326	EAVUx yS	EAVU was de–activated by an EAVU driver
S 374	N8H I	N8-H/N-AS cannot be re–parameterized
	N8H II	N8-H/N-AS cannot be re–parameterized
S 387	BUSSTECK	Local bus interface has been removed (only in connection with the N–AS local bus interface and system software release ≥ F03.00). The alarm is only issued at the central unit whose bus connector has been removed.
S 398	N8H I N8H II	N8-H/N-AS of ZE I/II has de–parameterized. Re–parameterization has been performed automatically.
S 800	XY → MR	Mode has changed from X/Y to M/R (X/Y represents any old mode)
S 801	XY → MB	Mode has changed from **X**/Y to M/B
S 802	XY → MP	Mode has changed from X/Y to M/P
S 803	XY → MF	Mode has changed from X/Y to M/F
S 804	XY → RM	Mode has changed from X/Y to R/M
S 805	XY → BM	Mode has changed from X/Y to B/M
S 806	XY → PM	Mode has changed from X/Y to P/M
S 807	XY → PP	Mode has changed from X/Y to P/P
S 808	XY → PF	Mode has changed from X/Y to P/F
S 809	XY → FM	Mode has changed from X/Y to F/M
S 810	XY → FP	Mode has changed from X/Y to F/P
S 811	XY → FF	Mode has changed from X/Y to F/F
S 812	BED: 1M	Operator input: CPU I becomes master
S 813	BED: 1P	Operator input: CPU I becomes passive
S 814	BED: 2M	Operator input: CPU II becomes master
S 815	BED: 2P	Operator input: CPU II becomes passive
S 816	SYNC SW	Keyboard input: Synchronize CPU I and II
S 817	SYNC HW	Synchronize by pressing the pushbutton on VKB
S 820	F-EINSYN	Hardware fault during synchronization
S 821	BGR-AUSB	Synchronization aborted; different module configuration
S 822	RAM-AUSB	Synchronization aborted; different user memory configuration
S 823	RAM P < M	Synchronization aborted; passive RAM < master RAM (if synchronization with different RAM configuration has been selected)
S 824	S-RAM I	Synchronization aborted; fault in CPU I system RAM
S 825	S-RAM II	Synchronization aborted; fault in CPU II system RAM
S 826	SYST-VER	Synchronization aborted; different system version
S 827	H235xxxx	Restart after system software change (xxxx = new system software version)
S 828	RAM P > M	Different RAM configuration; synchronized (if synchronization with different RAM size has been selected
S 829	SYST-WE	Different system software version; synchronized (selected by SA = 1) x in the following alarm texts indicates the EAVU number (x = 0 to 3); y indicates basic cabinet (y = G) or extension cabinet (y = E)
S 830	EAVUx yS	Incorrect jumper setting (different jumpers on I and II)
S 831	EAVUx yS	The EAVU is responsible for the same address range as another EAVU that has previously been checked
S 832	EAVUx yS	The EAVU has primary responsibility for the same group interrupt module word as another EAVU that has previously been checked
S 833	EAVUx yS	Bus fault (data path fault) in extension unit
S 834	EAVUx yS	24-V failure in extension unit
S 835	EAVUx yS	Internal EAVU fault (no 24–V failure) (When using a DG 235 diagnostic unit, the I&C alarm may also be issued though there is no EAVU fault. Acknowledge the I&C alarm without taking any further actions)
S 840	DAUERINT	Interrupt present for a too long time
S 842	EANK FEH	Defective EANK generation (fault on I/O bus interface module in basic cabinet)
S 843	EANK FEH	Defective EANK generation (fault on I/O bus interface module in extension cabinet)
S 844	INTHAEUF	Too many interrupts/interval (read register 2, bit 7 of an EAVU)
S 845	QVZ FEH	Fault in QVZ monitoring logic of CPU module
S 899	H-STATUS	Incorrect H mode in SB status register

Table 2.4 I&C alarms (continued)

The tests issuing the I&C alarms S 830 to S 843 are performed at intervals between 1 and 2 minutes. It is thus possible that it takes up to 2 minutes until an I&C alarm is issued again if the fault persists after it has been acknowledged.

2.7 Printout

The printers are connected to both CPUs via special cables with three connectors. Measures in the central unit guarantee that only the transmitter line of one operator input channel module per operator channel is active.

This means that only printouts from the master CPU are possible in asynchronous operation. These printouts are the same as in an AS 235 standard system.

3 Configuration

3.1 Difference between the AS 235 H and AS 235 Standard System Software

A program execution in the AS 235 H system is slower by approximately 5 % than in the AS 235 standard system. This reduced performance, which is caused by the hardware, must be taken into account when interpreting the Table “Memory assignment and execution time” in Chapter 9.4 of the “AS 235 Variant G” Description (C79000-T8076-C416).

Like in the standard system, the system execution time in the AS 235 H system is sliced into user–related time and system–related time (cf. Chapter 2.3.7.2 of the above–mentioned Description).

The system programs (Compiler and display processing, level 14) require additional execution time in an AS 235 H system:

– Except for updating, < 5 ms per second are required in each mode (= 0,5 % of the total execution time).
– Updating mode (M/B or B/M) requires < 50 ms/second (= 5 %).

This execution time is achieved at the expense of the overall execution time. As with the AS 235 standard system, at least 75 % of the overall execution time are thus available for user programs.

The AS 235 H system software requires approximately 250 bytes more space in the user memory.

Loading is aborted, and asynchronous operation begins if a fault occurs during loading in synchronous operation. Both CPUs clear their user memory contents.

Communication using PROGRAF via a serial interface with higher baud rates is disturbed during synchronization or in the event of a failure during synchronous operation. The last input must then be repeated.

3.2 Additional Functions

3.2.1 Function Flags in GB.ORPA

The system program sets the following flags in GB.ORPA:

Program flags	Meaning
GB.ORPA.150 = 0B = 1B	CPUs are not in redundant mode CPUs are in redundant mode (M/R or R/M)
GB.ORPA.151 = 1B	EAVU 0 in the basic cabinet is installed and has access to its extension unit (Extension unit no. 1 in normal configuration)
GB.ORPA.152 = 1B	EAVU 1 in the basic cabinet is installed and has access to its extension unit (Extension unit no. 2 in normal configuration)
GB.ORPA.153 = 1B	EAVU 2 in the basic cabinet is installed and has access to its extension unit (Extension unit no. 3 in normal configuration)
GB.ORPA.154 = 1B	EAVU 3 in the basic cabinet is installed and has access to its extension unit
GB.ORPA.155 = 1B	EAVU 100 in the extension cabinet is installed and has access to its extension unit (Extension unit no. 4 in normal configuration)
GB.ORPA.156 = 1B	EAVU 101 in the extension cabinet is installed and has access to its extension unit (Extension unit no. 5 in normal configuration)
GB.ORPA.157 = 1B	EAVU 102 in the extension cabinet is installed and has access to its extension unit (Extension unit no. 6 in normal configuration)
GB.ORPA.158 = 1B	EAVU 103 in the extension cabinet is installed and has access to its extension unit (Extension unit no. 7 in normal configuration)
GB.ORPA.159	Reserved for AS 235 H

Table 3.1 Flag meaning/assignment

3.2.2 Indication of a Failure in the I/O System (EAVU Driver Block)

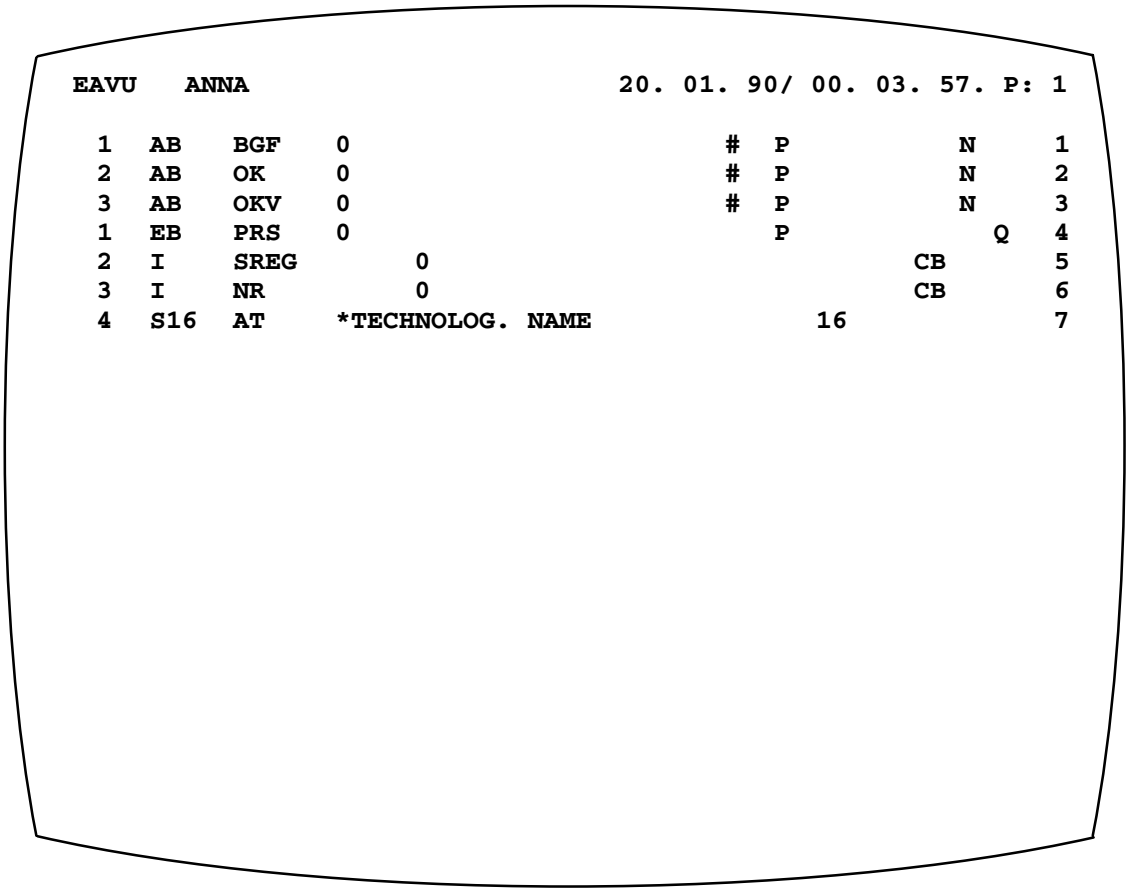


Fig. 3.1 Driver block list

The EAVU driver block (type no. 152) checks whether the associated EAVU has acknowledged (BGF = 0) and has access to its extension unit (OK = 1).

The EAVU number must be parameterized:

P,3,no; no = 0 ... 3 for EAVU 0 ... 3 in the basic cabinet
no = 100 ... 103 for EAVU 100 ... 103 in the extension cabinet

The OKV output transitions to 0 one cycle after the EAVU access to its extension unit has been interrupted. OKV transitions from 0 to 1 immediately after access has been re–established.

The outputs OK and OKV are used by XB blocks for activating or de–activating block sequence processing. This function enables driver blocks for I/O modules in an extension unit to be activated or de–activated. In a redundant I/O system, these switches are used for selecting the redundant values.

Interconnecting OK with an XB block prevents the subsequent driver blocks from indicating time–out if the associated EAVU fails or the extension unit voltage is switched off.

If OKV is interconnected with an XB block, the same circumstances cause the driver blocks to signal time–out once and to mark their outputs as being disturbed. Subsequently, they are not executed until the failure has been eliminated. This procedure has significant advantages with respect to the execution time.

The PRS (Peripheral reset signal) parameter is used for issuing a program–controlled reset of the I/O modules in individual extension units.

The EAVU addressed by the NR parameter is de–activated if the PRS parameter is 1. The associated I/O modules are reset. The reaction is as follows:

– The outputs of the output modules (binary/analog) are reset (depending on the ARS jumper)
– The closed–loop control module changes from mode C (compute) to mode A (automatic)
– 2–channel closed–loop control modules, backplane connector 2, CB signal to 0

The EAVU control over the I/O modules is activated and the reset signal for the I/O modules cancelled when the PRS input transitions from 1 to 0. Note that this reaction is not achieved by the value “0” at the PRS input but by the **transition** from “1” to “0”!

The EAVU is also activated and the reset signal for the I/O modules cancelled when the NR input is parameterized and PRS = 0.

The EAVU is not activated if the extension unit jumper configuration on the EAVU slot is inconsistent (see Chapter 2.5.1.2).

The state of an EAVU that has been de–activated by an EAVU driver (which has reset the associated I/O modules) will be retained until it is terminated by an EAVU driver. This effect must be noted when an EAVU driver is cleared or removed from an execution sequence.

An additional asterisk (*) next to “AUS” [OFF] in the “EAVU status display” screen display indicates that the EAVU has been de–activated by an EAVU driver (see Chapter 2.5.1.2).

The SREG input is used for writing into the EAVU control register. A decimal value is required for parameterization, invalid values will be rejected. Only values that are different from zero are transferred to the EAVU during each block execution (cf. EAVU description, C79000-T8076-C343).

A process–related name can be assigned in the AT parameter (display text).
Calling the driver block enables the EAVU block to be used for displaying the EAVU read register contents in hexadecimal representation:

EAVU,name;

```
 EAVU   ANNA                        *TECHNOLOG. NAME

EAVU-NUMMER NR=103


BAUGRUPPENFEHLER EAVU:  BGF=0

E/A-ZUGRIFF MOEGLICH:    OK=0

LESEREGISTER DER EAVU:  LR0=00
                        LR1=00
                        LR2=00
                        LR3=00
                        LR4=00
                        LR5=00
                        LR6=00
                        LR7=00

STEUERREGISTER:         SREG=  0
```

Fig. 3.2 EAVU driver block

3.2.3 Interrupt Processing

There are the following differences in interrupt processing between AS 235 H and AS 235 Standard:

– Alarm level 1 (cycle 1) is started when the CPUs enter asynchronous operation. This enables the user to initiate a program–controlled reaction to a loss of redundancy. GB.ORPA.150 contains the information whether or not the CPUs are redundant
(redundant = 1, not redundant = 0).

– The EAVUs set interrupt inhibition if, due to a peripheral fault, there are either too many interrupts or interrupts are present for a too long time. (Cf. EAVU module Description, C79000-T8076-C343).
The system software issues an I&C alarm (S 840 for permanent interrupt, S 844 for too many interrupts per time interval) if an interrupt inhibition occurs on one of the EAVUs. The system software terminates this inhibition after approximately 60 to 90 seconds.
The EAVU sets the inhibition again without delay if the fault persists, and interrupt processing is performed every 60 to 90 seconds.

4 Fault Handling

4.1 Specific System Software Test Routines

The system software contains test routines that facilitate early discovery of hidden hardware faults. Hidden hardware faults have no direct effect on the bus lines that are permanently monitored by comparator modules. Fault detection is thus independant of the user program. These test functions are repeated at intervals of less than 10 minutes.

The following test routines are carried out in addition to the tests performed in AS 235 Standard:

- CPU test
- memory test
- test of the functions in the I/O system
- test of all I/O comparator and switchover modules (EAVU)
- test of the N8-H/N-AS modules
- test of the comparator coupler module (VKB) (including test of the monitoring logic)
- test of the synchronization module

The optional system RAM block parity test (GB.ORPA.22) of the AS 235 Standard system is also possible in an AS 235 H system.

Faults in the I/O system are indicated by the I&C alarms S 830 to S 843 (see Chapter 2.6.3).

Faults detected by the other test routines trigger a comparator on the comparator coupler module (VKB) or the I/O comparator and switchover modules (EAVU). The reactions of these modules are described in Chapter 4.2.

4.2 Fault Reaction

If a discrepancy in synchronous operation, that has been caused by a hardware fault, is detected on the address, data, or control lines of the two CPUs, an interrupt in both CPUs initiates a fault finding diagnostic routine.

The following tests have been implemented in this diagnostic routine

– CPU test
– test of the 8–bit bus
– test of the operator input channel interface modules
– test of the I/O bus
– test of the I/O bus interface modules
– test of all I/O comparator and switchover modules (EAVU)
– test of the N8-H/N-AS
– memory test

Fault finding is terminated after a maximum of 50 ms. Three different results are possible:

1. The diagnostic routines cannot find a fault in either of the CPUs

   The master CPU retains mastership; the other CPU transitions to passive mode.

2. A diagnostic routine can locate a fault in its local CPU

   The master CPU enters failure mode and the standby CPU assumes mastership if the master CPU is faulty and in M/R or R/M state.
   The master CPU remains in master mode while the other CPU enters passive mode and clears its memory (that contains inconsistent data) if the master CPU is faulty and in M/B or B/M state.
   The non–master CPU transitions to failure mode if it contains the fault.

3. Both diagnostic routines locate a fault in their respective CPU

   The master CPU remains master, and the other CPU enters failure mode.
   (This result is very unlikely as it implies a double fault).

Alarm level 1 (cycle 1) is started when the CPUs enter asynchronous operation. This enables the user to initiate a program–controlled reaction to a loss of redundancy. GB.ORPA.150 contains the information whether or not the CPUs are redundant (redundant = 1, not redundant = 0).

The CPU goes to STOP, and the other CPU assumes mastership at once if the diagnostic routine finds a fatal hardware fault.

A fault in backup mode causes the backup CPU to perform a restart which clears the user memory. Fault finding in the backup CPU is not performed in this case.

Fault finding is not performed either if a fault occurs during loading in synchronous operation. Loading is aborted by the CPU which is not master and which clears its memory content.

The system responds to a fault after approximately 1 to 50 milliseconds (depends on the fault). The user program is not executed during this time which is required for executing fault finding routines (dead time).
Automatic synchronization after unsuccessful fault finding can be parameterized (see Chapter 2.5.1.1).

Since, in synchronous operation of CPU I, keyboard inputs are not read from BKA 2 (or, in synchronous operation of CPU II, keyboard inputs from BKA 1), the following I&C alarms can be issued after both CPUs have entered asynchronous operation:

CPU I signals: **SYST.E3 * S 331**
SYST.E3 * S 312

CPU II signals: **SYST.E2 * S 330**
SYST.E2 * S 312

This indicates a character overflow in the corresponding BKA.

It is thus possible that the last keyboard input of the corresponding operator input channel has not been received correctly. Input should then be repeated.

4.3 Fault Indications

An I&C alarm indicates a fault related change of the mode.

Example:

MR → FM * S 809

Fault in CPU I:

Mastership is transferred from CPU I to CPU II

The cause of the fault is not indicated, but can be viewed in an AS fault screen form (see Chapters 2.5.1.3 and 2.5.1.4).
An operator terminal at the automation system or a central configuring terminal is necessary for this function.

4.4 Fault Analysis

Chapters 2.5.1.3, 2.5.1.4 and 2.5.1.5 describe how fault information from the AS can be displayed.

Interpretation of the flags described in Chapters 2.5.1.3 and 2.5.1.4 can only be performed if the VKB and EAVU module descriptions are used (see AS 235 H Manual, Order No. C79000-G8076-C293).

Fault interpretation requires the flag screen forms to be interpreted in the following sequence:

1) **MP=3**: Date and time

2) **MP=5**: Columns 1 (”FEHLER ZE I”) [fault CPU I) and 2 (”FEHLER ZE II”) [fault CPU II]: If at least one of these columns contains a value that is different from 00, the cause of the synchronization fault has been detected by the software. With any other indication, proceed as follows:

3) **MP=3**: Columns 3 (”F-TYP ZE I”) [F–type CPU I] to 6 (”BGR ZE II”) [module CPU II]

4) **MP=5**: Columns 3 (”TYP-NAME”) to 8 (”VKB-REG. ADR.-BUS”)

5) **MP=4**: All columns

Steps 4 and 5, in particular, require system knowledge and can thus only be performed by a system expert.

4.5 Fault Elimination

A fault can normally only be eliminated by replacing the defective module.

The faulty CPU must be reset (RSOF or ZRS) in order to exit failure mode. This has no effect on the other CPU.

Test routines are executed during the subsequent start–up process. Once these routines have been passed, the CPU is in passive or master mode, depending on the mode of the other CPU (see Chapter 1.3 “Start–up Behavior”).

Please refer to the AS 235 H Instructions (C79000-B8076-C293) for further information.

5 Function Blocks

The two driver blocks PBE and PRA enable the use of the two testable binary input and output modules PBE and PRA which are particulary suitable for redundant systems. The use of the two modules in the AS 235 H is outlined in the following.

The driver blocks are described in Chapter 9.3 of the Description “AS 235 System Software Variant G” (see Section 1 of the Manual).

5.1 Testable Binary Input Module (PBE) 6DS1618-8CA

In contrast to other modules from the TELEPERM M module range, the PBE module offers special hardware fault detection procedures that enable swift elimination of hardware faults.

The module may be used in a 1–out–of–1, 1–out–of–2, or 2–out–of–2 structure.

– Two binary values from two different modules are read and ORed in a 1–out–of–2 structure.
– Two binary values from two different modules are read and ANDed in a 2–out–of–2 structure.

OR and AND interconnection of the binary values must both be provided by the user during configuration.

The module fault signal (BGF) from the driver blocks may alternatively be used for routing the two binary signals to one of the two driver blocks and modules.

The following example shows a 1–out–of–2 interpretation of 16 binary values that have been read by two redundant PBE drivers:

Explanation:

PBE.EIN1	is a driver
PBE.EIN2	is the driver that is redundant to PBE.EIN1
GB.EIN1.28	PBE.EIN1 has stored 16 binary values from this address onwards
GB.EIN2.36	PBE.EIN2 has stored 16 binary values from this address onwards
BG.AUS.54	The program section below stores the ORed values from both drivers from this address onwards.
SYSTEM.BWDZ	Converts 16 or 32 values of a binary data field into a bit sequence of an analog variable.

SYSTEM.DZBW Converts a bit sequence of an analog variable with 2 or 4 bytes into 16 or 32 values of a binary data field. Both programs are explained in the Description C79000-G8076-C416.

The output values from the driver blocks are only ORed if both driver blocks are faultless. The 16 binary values from the faultless module are stored from GB.AUS.54 onwards if this is not the case.

A simultaneous fault in both modules is excluded.

```
IF NOT PBE.EIN1.BGF;
THEN;                    PBE.EIN1 is faultless
  MUX GB.EIN1;
  CALL SYSTEM.BWDZ;
  GIVE 0,28;             Convert 16 binary values into a binary number
  ;                      from GB.EIN1.28 onwards
  TAKE LA0;              Store the result in LA0
  ;
  IF NOT PBE.EIN2.BGF;
  THEN;                  PBE.EIN2 is faultless
    MUX GB.EIN2;
    CALL SYSTEM.BWDZ;
    GIVE 0,36;           Convert 16 binary values into a binary number
    ;                    from GB.EIN1.36 onwards
    TAKE LA1;            Store the result in LA1
    ;
    LA0 ODR LA1=:LA0;    OR both values, and store result in LA0
  END IF;
ELSE;                    PBE.EIN1 is faulty
  MUX GB.EIN2;
  CALL SYSTEM.BWDZ;
  GIVE 0,36;             Convert 16 binary values into a binary number
  ;                      from GB.EIN1.36 onwards
  TAKE  LA0;             Store the result in LA0
  ;
END IF;
;
MUX GB.AUS;
CALL SYSTEM.DZBW;
GIVE 0,54,LA0;           Output 16 binary values
;                        from GB.AUS.54 onwards
```

Please observe the notes regarding jumper setting that are given in the instructions for the testable binary input module (PBE), Order No. C79000-B8076-C131.

The following switch and jumper settings are required if the module is used in the AS 235/AS 235 H systems:

– Switches S1 to S4:	1	(no interrupt triggering)
– Plug–in jumper X50:	1 – 16	open
	2 – 15	open
	3 – 14	open
	4 – 13	open
	5 – 12	don't care
	6 – 11	open
	7 – 10	inserted
	8 – 9	inserted

5.2 Testable Relay Output Module (PRA) 6DS1606-8BA

In contrast to other modules from the TELEPERM M module range, the PRA module offers special functions that enable complete detection of module faults, including contact monitoring functions.

The module may be used in a 1–out–of–1, 1–out–of–2, or 2–out–of–2 structure. The module's relay outputs must be wired to the actuators according to the application.

– The 1–out–of–1 structure enables hardware defects to be detected immediately and thus to be eliminated rapidly.
– The 1–out–of–2 structure additionally makes it possible that the discrete value "1" or ON can always be issued to the actuator, even if there is a hardware defect on **one** module.

  This means:

  One module controls the actuator correctly if the incorrect output signal from the other module is "0" or OFF.

  If, in contrast, the incorrect output signal from a module is "1" or ON, the actuator is set to "1" or ON irrespective of the state of the related output signal from the faultless module.

Caution

If a channel is used in a 1–out–of–2 structure, a fault value of 0B must be selected if the freeze bit of the master driver (EINF = 0B) has been reset.
This means: The bit that has been allocated to this channel in the corresponding fault default value (VWF1, VWF2, VWF3, VWF4) of the master driver must be reset.

– In addition to immediate fault detection, the 2–out–of–2 structure guarantees that outputting a binary value "0" or OFF to the actuator is always possible after a hardware malfunction has occurred on **one** module.

  This means:

  The actuator position is "0" or OFF if an incorrect output signal from a module is "0" or OFF, irrespective of the state of the related output signal from the faultless module.

  If, in contrast, the incorrect output signal from a module is "1" or ON, the other module sets the actuator to the correct position.

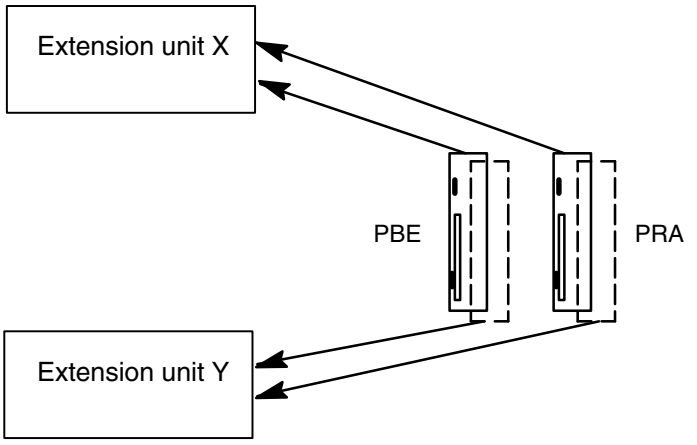
The interconnection structures 1–out–of–2 and 2–out–of–2 require the output signal from a user structure to be issued via two driver blocks on two PRA modules that must be installed in two different extension units. The connection instructions for the individual connection types are contained in the Instructions of the testable relay output module (PRA), Order No. C79000–B8076–C160.

Please observe the instructions regarding jumper setting that are also given in these Instructions.

The following jumper settings are required if the modules are used in AS 235/AS 235 H systems:

–	Plug–in jumper X29:		inserted	Watchdog circuit active
–	Plug–in jumper X11:	1 – 2	inserted	Load current must flow from the common contact to the NC or NO contact
		:		
		31 – 32	inserted	
–	Plug–in jumper X4:	2 – 3	inserted	Tripped fuse monitoring ON
–	Plug–in jumper X7:	2 – 3	inserted	
–	Plug–in jumper X31:	1 – 2	inserted	Only valid for 2–out–of–2 structure **and** utilization as a slave module
	:	:	:	
	:	:	:	
	X46:	1 – 2	inserted	
–	Plug–in jumper X31:	2 – 3	inserted	Valid for any other utilization
	:	:	:	
	:	:	:	
	X46:	2 – 3	inserted	

5.3 Redundant Utilization of the Modules



In redundant applications, PBE and PRA **must** both be installed in **different** extension units.

Fig. 5.1 Redundant utilization of PBE and PRA

If two PBE modules are used in a redundant structure, a transducer in the process must be connected to one channel of each PBE module. The driver blocks must also exist twice.

It two PRA modules are used in a redundant structure, two driver blocks issue an output signal to the two modules.

The wiring instructions are contained in the above–mentioned PRA Instructions.

Appendix

Upgrading instructions for memory module 6DS1844–8FA and system software version G

The following description assumes that the H operating status at the beginning of the upgrading procedure is M/R (modify accordingly for R/M).

1 Upgrading of hardware

Initial status: Memory module 6DS1837-8xA in CPU I and CPU II,
System software version F with release ≥ F03.02 in CPU I and CPU II,
H operating status M/R

Carry out the upgrading in the following steps:

– Switch off CPU II (⇒ H operating status M/F) and replace its memory module 6DS1837-8xA by 6DS1844-8FA.
– Boot CPU II using the system software of CPU I.
– If CPU I has a memory configuration of 1 or 2 MByte: activate "**`RA=1;`**" in the first screen form of SYST.HBED.
– Synchronize from the keyboard ("**`EE=1;`**") or using the key (BU) on the front panel of the VKB (⇒ H operating status M/R).
– Switch off CPU I (⇒ H operating status F/M) and replace its memory module 6DS1837-8xA by 6DS1844-8FA.

If, in addition to upgrading of the hardware, the system software is to be upgraded **immediately** to version G: continue with 3.

2 Generation of redundant H operating status with retention of system software version F

Initial status: Memory module 6DS1844-8FA in CPU I and CPU II,
System software version F with release ≥ F03.02 in CPU II,
H operating status F/M

Generate the redundant H operating status using the following steps:

– Boot CPU I using the system software of CPU II (⇒ H operating status P/M).
– If the original configuration of the AS with respect to the user RAM was 1 or 2 MB: activate "**`RA=1;`**" in the first screen form of SYST.HBED.
– Synchronize from the keyboard ("**`EE=1;`**") or using the key (BU) on the front panel of the VKB (⇒ H operating status R/M).

Upgrading of the memory module 6DS1844-8FA has thus been terminated.

If upgrading to system software version G is to be carried out: continue with 3.

3 Upgrading of the system software to version G

Initial status: Memory module 6DS1844-8FA in CPU I and CPU II,
System software version F with release ≥ F03.02 only in CPU II or in CPU I and CPU II,
H operating status F/M or R/M

Carry out the upgrading in the following steps:

– Boot CPU I using the system (⇒ H operating status P/M).

– Activate "**`SA=1;`**" and "**`RA=1;`**" in the first screen form of SYST.HBED.

– Synchronize from keyboard ("**`EE=1;`**") or using the key (BU) on the front panel of the VKB. The AS 235 H then temporarily assumes the H operating status B/M and then changes to the H operating status M/P in which CPU I carries out a start–up.

– Boot CPU II using system software version G.

– Synchronize from keyboard ("**`EE=1;`**") or using the key (BU) on the front panel of the VKB (⇒ H operating status M/R).

The upgrading to software version G with memory module 6DS1844–8FA has now been terminated.

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